A Precise 90° Quadrature OTA-C Oscillator Tunable in the 50–130-MHz Range

Bernabé Linares-Barranco, Teresa Serrano-Gotarredona, Juan Ramos-Martos, Joaquín Ceballos-Cáceres, José Miguel Mora, and Alejandro Linares-Barranco

***Abstract*—We present a very-large-scale integration continuous-time sinusoidal operational transconductance amplifiers quadrature oscillator fabricated in a standard double-poly 0.8-μm CMOS process. The oscillator is tunable in the frequency range from 50 to 130 MHz. The two phases produced by the oscillator show a low-quadrature phase error. A novel current-mode amplitude control scheme is developed that allows for very small amplitudes. Stability of the amplitude control loop is studied as well as design considerations for its optimization. Experimental results are provided.**

***Index Terms*—Amplitude control, analog very large-scale integration (VLSI), g_mC, impedance probe, multiphase oscillators, operational transconductance amplifiers (OTA)-C, oscillator stability, phase noise, quadrature oscillators, sinusoidal oscillators, transconductance-capacitance oscillators.**

I. Introduction

QUADRATURE oscillators are key building blocks in many signal-processing circuits for telecommunication and instrumentation applications. Many times, square-wave quadrature oscillators are satisfactory. However, and specifically for instrumentation, most of the times, one requires two continuous-time sinusoidal signals at 90° phase shift, and with extremely low error in the phase difference. The quadrature oscillator described in this paper was developed for its possible use within a soil-impedance measurement system. Soil characteristics such as humidity and salinity can be inferred from the reactive and resistive components of its impedance, when measured at frequencies in the range of 50–100 MHz [1]–[4]. Furthermore, other characteristics, properties, and even composition can be inferred by measuring an impedance profile as a function of frequency.

Small and cheap soil-impedance probes can be used to spread over large agricultural fields can be used to sense and monitor the soil characteristics over time and optimize the use of (many times limited) water resources. A soil-impedance probe can be realized using a conventional impedance bridge, as shown in Fig. 1. The scheme uses two sinusoidal signals with a 90° phase shift. Such a phase shift can be obtained from a single sinusoid by applying it to a passive network that would introduce the extra 90° phase shift [5]. However, this can be done for a fixed frequency only. In our case, we would like to sweep the frequency over a very wide range [1]–[4]. Consequently, we will consider the possibility of designing a sinusoidal quadrature oscillator tunable over the required frequency range. In the scheme shown in Fig. 1 one phase is applied to the impedance bridge, while both phases multiply the resulting voltages V_1 and V_2 of the impedance bridge, producing error signals e_1 and e_2. In a properly constructed auto-nulling system [6], the "signal-processing" block will generate two control signals c_1 and c_2 (which control the internal and calibrated resistor R_p and capacitor C_p), such that V_1 and V_2 become identical. At this point, the value of resistance R_p equals the resistive component of the external unknown impedance for the present frequency, while the value of capacitance C_p provides the reactive part for this frequency. Repeating this for different frequencies provides a resistive and reactive impedance profile of the present soil.

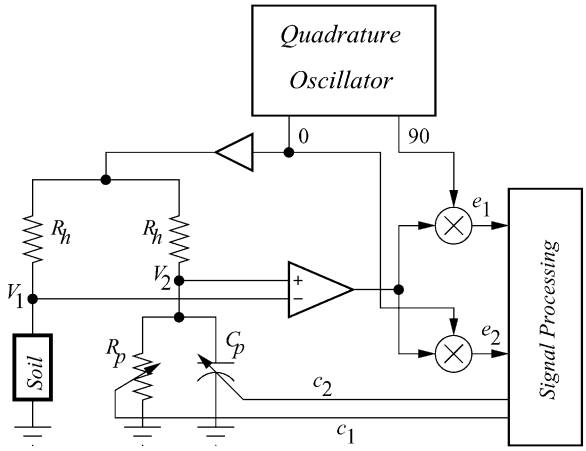


Fig. 1. Impedance bridge for measurement of unknown impedance values.

Soil probes should be very compact. Consequently, one would like to include all the sensing, processing, and communication circuitry within a single very-large-scale integration (VLSI) chip. Power consumption is important, but not extremely critical: the probes would stay normally in a "stand-by" or "sleep" mode and perform an impedance measurement during a few (or a fraction of) seconds once every few hours. For a VLSI continuous-time quadrature sinewave oscillator in the 50–100-MHz frequency range, the ideal circuit design technique is operational transconductance amplifiers (OTA)-C [7]–[9]. OTAs provide good frequency response above 100 MHz at reasonable power consumptions, and do not require the use of resistors for assembling oscillators [13], [14].

The time constants of OTA-C oscillators and filters depend on the ratio between a transconductance gains and capacitances.

Manuscript received February 20, 2003; revised November 13, 2003. This paper was recommended by Associate Editor A. Baschirotto.

The authors are with the Instituto de Microelectrónica de Sevilla, 41012 Seville, Spain (e-mail: bernabe@imse.cnm.es).

Digital Object Identifier 10.1109/TCSI.2004.823673

1057-7122/04$20.00 © 2004 IEEE

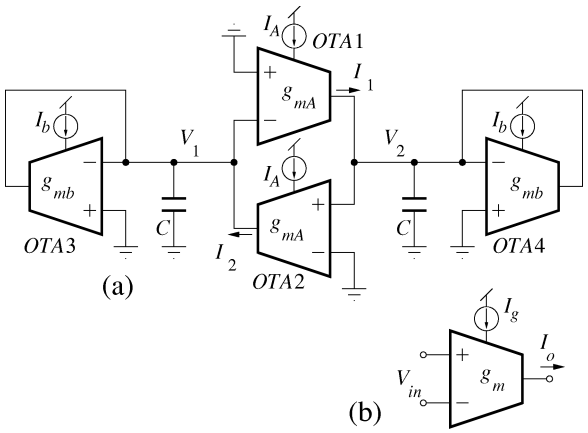


Fig. 2. (a) OTA-C quadrature oscillator structure. (b) OTA symbol.

Such a ratio suffers from important temperature and process variations for VLSI implementations (up to 20%–30%, for standard CMOS processes). Consequently, if precise time constants are required, it becomes necessary to resort to locking-to-reference signals for oscillators [13] or to add frequency tuning loops for filters [8]–[13]. In the past decades, important contributions to tuning of OTA-C circuits have been made, and a variety of solutions are readily available in the literature [8]–[12]. In this paper, we will just describe how to implement a current-controlled quadrature oscillator but without including any time-constant tuning technique.

The paper is organized as follows. Section II describes the quadrature oscillator structure capable of producing precise 90° shifted signals over a wide frequency range. In Section III, an efficient and fast amplitude tuning loop is shown that can control the amplitude of oscillations to very small amplitudes. Section IV analyzes the conditions under which the amplitude control is stable. Section V describes the circuit blocks and Section VI shows experimental results.

II. Quadrature Oscillator Structure

The objective is to obtain a sinusoidal oscillator with two phases at 90° difference, tunable in the range 50–100 MHz, and capable of producing small amplitudes to minimize distortion. The chosen circuit design technique is OTA-C [7]–[13] and a proper oscillator structure is shown in Fig. 2(a). The output current I_o of an OTA [see Fig. 2(b)] can be expressed in the frequency domain as [13], [14]

$$\begin{aligned} I_o(s) &= V_{in}(s) g_m(s) \\ g_m(s) &= g_{mo}\left(1 - \frac{s}{\omega_{mo}}\right) \end{aligned} \tag{1}$$

where g_{mo} is its dc transconductance gain and ω_{mo} a high-frequency zero that models phase shift effects. Both parameters g_{mo} and ω_{mo} will depend on the OTA bias current I_g. Note that for the structure in Fig. 2(a) the OTA1 and OTA2 output currents I_1 and I_2 "see" the same impedances at nodes V_1 and V_2. Let us call this impedance $Z_b(s)$

$$\begin{aligned} V_1(s) &= I_2(s) Z_b(s) \\ V_2(s) &= I_1(s) Z_b(s). \end{aligned} \tag{2}$$

On the other hand, the dependence of I_1 on V_1 is identical to that of I_2 on V_2, except for a change in sign

$$\begin{aligned} I_1(s) &= -g_{mA}(s) V_1(s) \\ I_2(s) &= g_{mA}(s) V_2(s). \end{aligned} \tag{3}$$

Consequently

$$\begin{aligned} V_1(s) &= Z_b(s) g_{mA}(s) V_2(s) \\ V_2(s) &= -Z_b(s) g_{mA}(s) V_1(s) \end{aligned} \tag{4}$$

independently of the specific form of $Z_b(s)$ and $g_{mA}(s)$, of any parasitics or nonidealities, as long as everything is symmetric. The solutions for (4) are either $V_1 = V_2 = 0$ or

$$V_1(s) = \pm j V_2(s). \tag{5}$$

Therefore, the arrangement of Fig. 2(a) will guarantee a 90° phase shift between voltages V_1 and V_2, and also between currents I_1 and I_2.

Using the OTA model of (1) in the oscillator structure of Fig. 2(a) yields the following frequency-domain characteristics equation for the oscillator

$$\begin{aligned} s^2 + bs + \omega_o^2 &= 0 \\ b &= 2\frac{g_{mb}(C - C_b) - g_{mA} C_A}{(C - C_b)^2 + C_A^2} \\ \omega_o^2 &= \frac{g_{mA}^2 + g_{mb}^2}{(C - C_b)^2 + C_A^2} \end{aligned} \tag{6}$$

where

$$\begin{aligned} C_A &= \frac{g_{mA}}{\omega_A}, && \omega_A \text{ is the high-frequency zero of OTA } g_{mA} \\ C_b &= \frac{g_{mb}}{\omega_b}, && \omega_b \text{ is the high-frequency zero of OTA } g_{mb}. \end{aligned} \tag{7}$$

When the oscillator produces stable amplitudes, then, $b = 0$, which implies that

$$\begin{aligned} g_{mb} &= g_{mA}\frac{C_A}{C - C_b} \\ \omega_o &= \frac{g_{mA}}{C - C_b}. \end{aligned} \tag{8}$$

As will be explained in the Section III, we will implement an automatic-gain-control (AGC) scheme that tunes the bias current I_b of OTA3 and OTA4 to set continuously $b = 0$ and maintain constant amplitude oscillations. The AGC loop will make transconductance g_{mb} be a function of the oscillator amplitude, through I_b

$$g_{mb} = g_{mb}(I_b(A)) = f(A). \tag{9}$$

Consequently, term b in (6) depends on the oscillator amplitude $b(A)$ through g_{mb}. Assuming this function is instantaneous,[1] it must satisfy the following conditions to yield a stable amplitude AGC loop [15].

1) There is an amplitude A_o for which $b(A_o) = 0$. This will be the steady-state oscillation amplitude.
2) For $A = 0$, it must be $b(0) < 0$, so that the poles of (6) have positive real part and the oscillator self-starts.
3) Function $b(A)$ must be a monotonic increasing function in the range from $A = 0$ to $A = A_{\max}$, the maximum possible expected amplitude.
4) At $A = A_o$ the derivative of b with respect to A should be strictly positive

$$\left.\frac{db}{dA}\right|_{A=A_o} > 0 \tag{10}$$

to assure stable amplitude control.

Term b depends on A through g_{mb}, which is controlled by I_b. Assuming that I_b is linear with A, with a positive proportionality constant, and the OTAs made with conventional differential pairs with I_b being their tail current (g_{mb} is proportional to $\sqrt{I_b}$); then, g_{mb} is monotonically increasing with A. Under these circumstances, the condition in (10) can also be stated as

$$\left.\frac{db}{dg_{mb}}\right|_{g_{mb}=g_{mbo}} > 0 \tag{11}$$

where g_{mbo} is the value of g_{mb} for which $b = 0$, which is actually given in (8). Using (6) in (11) results in the condition

$$\frac{db}{dg_{mb}} = 2\frac{C - C_b}{(C - C_b)^2 + C_A^2} > 0 \Leftrightarrow C > C_b. \tag{12}$$

Therefore, there is a minimum value of C which is required to obtain a stable amplitude AGC loop for the oscillator structure in Fig. 2(a).

III. Oscillator Amplitude Control Loop

When one uses the differential pair tail bias current to tune the OTA transconductance (and consequently, the oscillator frequency), it turns out that the available linear range of the OTA input-to-output transfer curve is highly dependent on that current (if it is biased in strong inversion). Using the MOS square law transistor model [16] for transistors M_1 and M_2 in Fig. 3(a), $I_{1(2)} = \beta_A(V_{1(2)} - V_S - V_T)^2$ yields

$$I_o = I_1 - I_2 = g_{mA}\Delta V\sqrt{1 - \frac{\beta_A}{2I_A}\Delta V^2} \tag{13}$$

where $\Delta V = V_1 - V_2$ and $g_{mA} = \sqrt{2\beta_A I_A}$. For $\Delta V = \pm\sqrt{I_A/\beta_A}$, the output current saturates at $I_o = \pm I_A$. Consequently, the range $\pm\sqrt{I_A/\beta_A}$ is dependent on the tail bias current, which also controls g_{mA}. Fig. 3(b) shows I_o versus ΔV for different values of I_A, while Fig. 3(c) shows the corresponding derivatives, i.e., g_m. These figures have been obtained by simulations with the AMS 0.8-μm CMOS models for an NMOS differential pair of size $W = 20$ μm, $L = 0.8$ μm, while sweeping the tail bias current from 5 μA to 40 μA. In Fig. 3(b), the slope of I_o versus ΔV becomes zero at $v_L = \pm\sqrt{I_A/\beta_A}$. At this point,

[1]As we will see in Section III, this function is not instantaneous and further stability conditions need to be addressed.

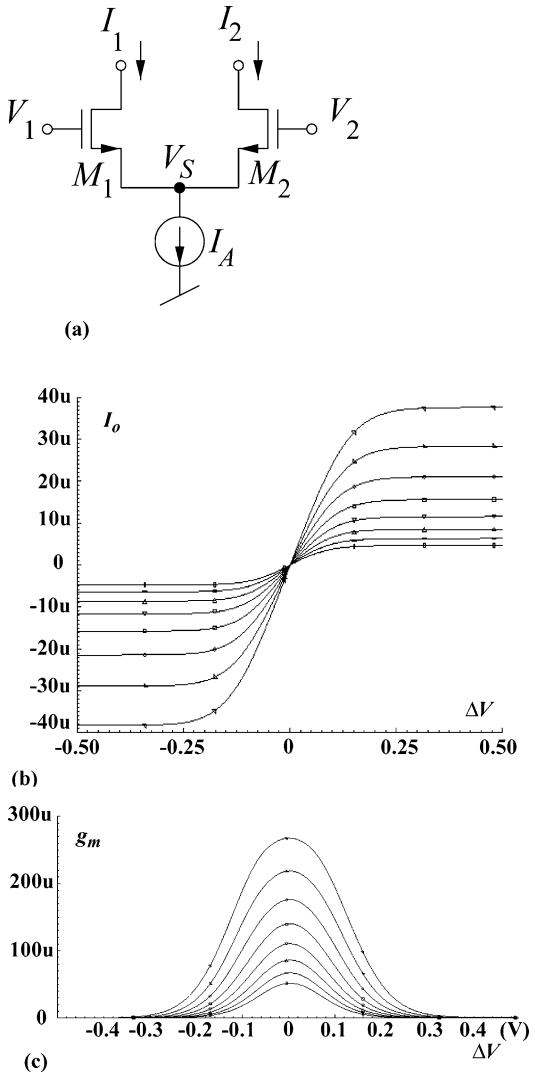


Fig. 3. Conventional differential pair. (a) Schematics. (b) Simulated output current. (c) Derivative or large-signal transconductance.

I_o saturates to $\pm I_A$. The linear range of the OTA can be considered to be a fraction of this voltage. In our case, we decided to set the amplitude in the current domain by adjusting the OTA output current amplitude to be 1/5 of bias current I_A. Consequently, the voltage linear range can be obtained by setting $I_o = I_A/5$ in (13) and solving for $\Delta V = v_l$ with $\beta_A = g_{mA}^2/(2I_A)$

$$v_l = \pm\sqrt{2 - \frac{4\sqrt{6}}{5}}\frac{I_A}{g_{mA}} = \pm\frac{1}{4.975}\frac{I_A}{g_{mA}} \approx \pm\frac{1}{5}\frac{I_A}{g_{mA}}. \tag{14}$$

This way, when the oscillating waveforms stabilize, the OTA experiences current excursions in the same fraction of the curves in Fig. 3(b), independently of the actual g_{mA} value, thus assuring always the same nonlinearity contribution. This will keep, in principle, the distortion at the same value, independently of frequency.

Equation (14) refers to the linear range of OTA1 and OTA2 in Fig. 2(a). For OTA3 and OTA4, we need to substitute the oscillations peak voltage in (14) into the I/V transfer curve of OTA3 and OTA4

$$I_{ob} = g_{mb}v_l\sqrt{1 - \frac{\beta_b}{2I_b}v_l^2} \tag{15}$$

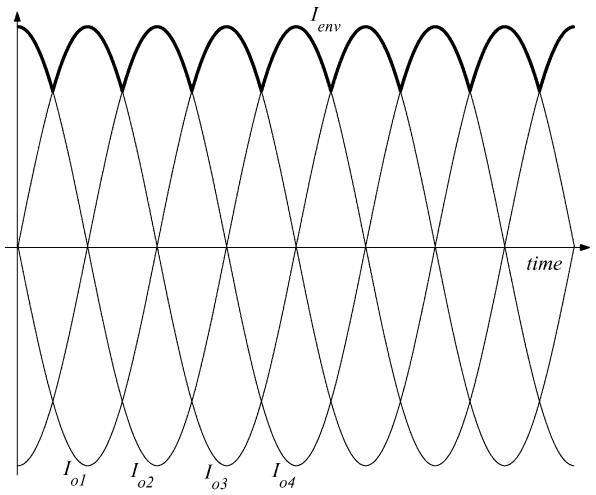


Fig. 4. Input and output waveforms for the MAX circuit.

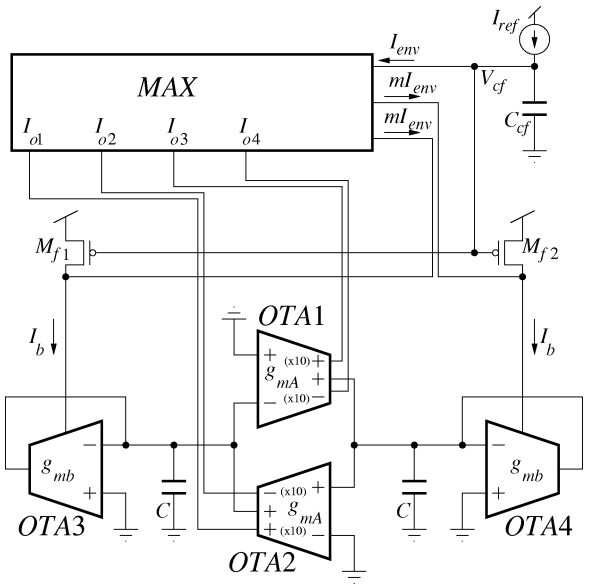


Fig. 5. Complete OTA-C quadrature oscillator with current-mode amplitude control loop.

to obtain the peak output current for these OTAs. Using (8) with (14) and (15), yields

$$\frac{I_{ob}}{I_b} = \frac{1}{5}\frac{\beta_b}{\beta_A}\frac{C-C_b}{C_A}\sqrt{1-\left(\frac{1}{10}\frac{\beta_b}{\beta_A}\frac{C-C_b}{C_A}\right)^2} \tag{16}$$

which is also a constant number, independent of frequency and transconductances. The extra freedom degree of β_b allows to set this fraction to a sufficiently low value (like 1/5) so that OTA3 and OTA4 also stay always within the same fraction of nonlinearity, introducing a constant distortion like OTA1 and OTA2.

In summary, the oscillator amplitude control loop needs to do the following:

a) extract the peak output currents of OTA1 and OTA2;
b) maintain it equal to 1/5 of bias current I_A which sets the oscillation frequency.

In order to achieve these goals, we provided OTA1 and OTA2 with two extra output currents: a copy of its original output current and an inverted copy. This way, we will have four currents of the same frequency and amplitude but with phases 0°, 90°, 180°, and 270°. These four phases' current signals can then be fed to a four-input current-mode MAX circuit to extract the instantaneous envelope of the oscillating signal, as illustrated in Fig. 4. The output of the MAX circuit $I_{\rm env}$ can then be compared against a reference current $I_{\rm ref} = (1/5)I_A$ to generate an error signal that controls I_b until oscillations stabilize at amplitude $(1/5)I_A$. The oscillator with this amplitude control scheme is depicted in Fig. 5. The difference between the MAX circuit output $I_{\rm env}$ and $I_{\rm ref}$ is integrated onto capacitor C_{cf}, whose voltage V_{cf} controls the gate of transistors M_{f1} and M_{f2}. The drain current of these transistors contributes to OTA3 and OTA4 bias current I_b. Also, a fraction of the MAX circuit output $mI_{\rm env}(|m| < 1)$ contributes to control current I_b. This introduces a zero in the integration operation of C_{cf} for stability purposes [13], [17], [18], which is explained in more detail in the Section IV.

IV. Stability of Amplitude Control Loop

Consider the time-domain version of (6)

$$\frac{d^2I_o(t)}{dt^2} + b(t)\frac{dI_o(t)}{dt} + \omega_o^2 I_o(t) = 0 \tag{17}$$

where $I_o(t)$ can be any of the four current phases in Fig. 5. Note that (17) can be used to describe any generic second order continuous-time oscillator. If $b(t) = b_o$ is constant, the solution to (17) is

$$I_o(t) = i_A(t)\cos(\omega t + \varphi) \tag{18}$$

with $\omega = \omega_o^2 - b_o^2/4$ and

$$i_A(t) = i_A(t_o)e^{-(b_o t/2)}. \tag{19}$$

The amplitude increases or decreases exponentially (depending on the sign of b_o), except if $b_o = 0$ in which case it remains stable at its initial value. On the other hand, if $b(t)$ is controlled by some means such that $b(t)$ changes at a much slower rate than $I_o(t)$ and such that it suffers very small variations around $b = 0$, then, we may assume that the oscillator amplitude $i_A(t)$ is kept around a constant value i_{Ao}, and that the oscillating frequency ω can be considered constant for practical purposes. Under these conditions, substituting (18) into (17) yields the following coefficients for the cosine and sine terms, which must be identically zero:

$$\frac{d^2i_A(t)}{dt^2} + b(t)\frac{di_A(t)}{dt} + (\omega_o^2 - \omega^2)i_A(t) = 0$$
$$2\frac{di_A(t)}{dt} + i_A(t)b(t) = 0. \tag{20}$$

From the second it follows that

$$i_A(t) = i_A(t_o)\exp\left(-\frac{1}{2}\int_{t_o}^{t} b(t)dt\right). \tag{21}$$

Let us choose t_o such that $i_A(t_o) = i_{Ao}$. When the amplitude $i_A(t)$ is close to i_{Ao} (either for a stable or unstable AGC loop), then, $b(t)$ is very close to zero, as well as the integral in (21).

Consequently, the exponential in (21) can be approximated by its first-order Taylor series expansion

$$i_A(t) \approx i_{Ao}\left(1 - \frac{1}{2}\int_{t_o}^{t} b(t)dt\right) = i_{Ao} + i_a(t) \tag{22}$$

where $i_a(t)$ is the "small-signal" amplitude at $i_A(t)$. In the frequency domain $i_a(t)$ will be

$$I_a(s) = -\frac{i_{Ao}}{2}\frac{b(s)}{s} \tag{23}$$

This expression is a very interesting result because it allows to write in the s domain (i.e., with a linear system description) the inherently complicated and nonlinear relationship between $b(t)$ and amplitude of $I_o(t)$ in (17). To our knowledge, this result was already known at least in 1974 by Vannerson and Smith [19], although derived in a more rudimentary way and with more restrictive assumptions.

The output of the MAX circuit has a continuos component and a ripple component (see Fig. 4). Let us assume the ripple component is filtered out by the AGC circuitry. Then, in general, the continuos component can be separated into the steady-state dc part I_{envo} and a small-signal time varying part $i_{\text{env}}(t)$. This small-signal part ($I_{\text{env}}(s)$ in the s-domain) will be a delayed and attenuated version of the instantaneous oscillator amplitude ($I_a(s)$ in the s domain)

$$I_{\text{env}}(s) = \rho I_a(s)(1 - s\tau_{\text{env}}) \tag{24}$$

where $1 > \rho > 0$ is the attenuation and time constant τ_{env} characterizes the delay.

The input signal of an amplitude control loop is the one that sets the amplitude externally. In our case, this signal is I_{ref}. Consequently, at capacitor C_{cf} we can write

$$sC_{cf}V_{cf}(s) = I_{\text{ref}}(s) - I_{\text{env}}(s). \tag{25}$$

If transistors M_{f1} and M_{f2} are described by their small-signal transconductance g_{mf}, then

$$I_b(s) = -g_{mf}V_{cf}(s) + mL_{\text{env}}(s). \tag{26}$$

The dependence of term $b(s)$ in (23) with $I_b(s)$ can be obtained from (6), where b is expressed in terms of g_{mb}, the transconductance of OTA3 and OTA4 controlled by I_b. Transconductance g_{mb} is proportional to the square root of I_b (for a conventional differential pair based OTA biased in strong inversion saturation). For small signals, $g_{mb}(s)$ will be proportional to $I_b(s)$, and so will be $b(s)$

$$b(s) = \alpha I_b(s). \tag{27}$$

Equations (23)–(27) describe completely in the s domain (small signal) the amplitude control loop of the circuit in Fig. 5. Solving these equations yields

$$\frac{I_a(s)}{I_{\text{ref}}(s)} = \frac{\frac{1}{\rho}}{1 + sk_2 + s^2k_1}$$
$$k_1 = \frac{2\tau_f}{\alpha\rho i_{Ao}} - m\tau_{\text{env}}\tau_f$$
$$k_2 = m\tau_f - \tau_{\text{env}} \tag{28}$$

where $\tau_f = C_{cf}/g_{mf}$. Stability is guaranteed for $k_1 > 0$ and $k_2 > 0$. Parameters m and τ_f have to be chosen so that k_1 and k_2 are positive for worst case α, ρ, i_{Ao} and τ_{env}. In summary, the stability conditions are

$$m > \frac{\tau_{\text{env}}}{\tau_f}$$
$$m < \frac{2}{\alpha i_{Ao}\rho\tau_{\text{env}}}. \tag{29}$$

The top inequality is amplitude independent, while the bottom one needs to be adjusted for maximum oscillator amplitude i_{Ao}. Note that depending on the circuit chosen for the envelope detector (or MAX circuit), τ_{env} and ρ may be also functions of i_{Ao}. Making $m = 0$ yields an unstable control loop. Therefore, the "zero" in integrator C_{cf} is required for stability. In the case of the circuit in Fig. 5 this "zero" is introduced by adding a scaled version of I_{env} to I_b.

Section V.D includes simulations illustrating the AGC performance, including estimations of the different parameters. Also, Appendix A develops on further considerations that provide hints on how to optimize the different AGC loop parameters for optimum transient responses. The principles in this Section have also been applied to the gigahertz range RF oscillators [17].

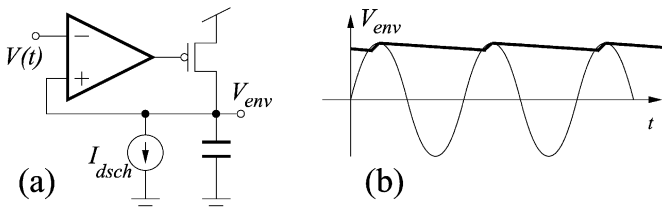


Fig. 6. Conventional peak detector circuit. (a) Schematics. (b) Input and output waveforms.

V. Description of Circuit Blocks

A. Four-Phase MAX Circuit Envelope Detector

An ideal envelope detector circuit should provide the envelope of an oscillating signal with zero delay and zero error in amplitude value: if the oscillating signal is $V(t) = A(t)\sin(\omega t + \varphi)$ the envelope detector output should be $A(t)$. Traditional peak detectors compare the instantaneous signal amplitude $V(t)$ against a peak value stored on a capacitor (see Fig. 6). If the amplitude exceeds the stored value, extra charge is added to the capacitor until ts voltage V_{env} equals the present instantaneous amplitude $V(t)$. This will allow the peak detector to follow a sudden increase in amplitude. In order for the circuit to be able to follow a decrease in amplitude, the capacitor is permanently discharged at a slower rate. The lower this rate, the less the ripple available at the output, but the slower its response to a decrease in amplitude. Also, if the signal frequency changes, ripple changes as well as time response to an amplitude decrease, unless I_{dsch} is changed accordingly with signal frequency. Also, note that in the optimum case, the minimum delay is equal to one signal period because until the next peak arrives the circuit is not aware of a change in peak value.

An interesting envelope detector alternative for multi phase oscillators are those that select the maximum of all available phases [19]. These circuits respond within a fraction of the period and detect equally fast an increase or decrease in amplitude, and independently of the size of the amplitude step or

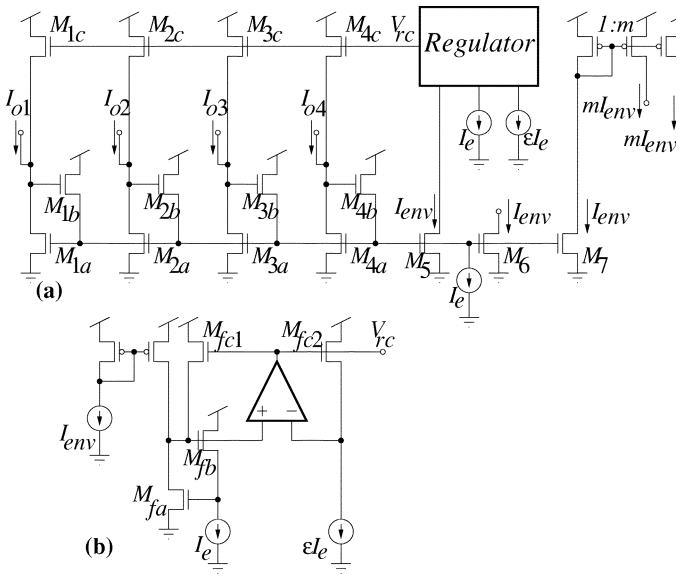


Fig. 7. (a) MAX circuit schematics. (b) Detail of regulator circuit.

signal frequency. Since our oscillator can provide four phases, we can use a four-input MAX circuit. The MAX circuit used is shown in Fig. 7. It is based on the classic Lazzaro [20] winner-takes-all circuit. Assume NMOS transistors M_{1c}-M_{4c} are OFF. The four-input currents I_{o1}-I_{o4} make transistors M_{1b}-M_{4b} compete for bias current I_e. The maximum current I_{oj} will make the gate-to-source voltage of its input branch transistor M_{jb} adjust to drive all (or most) of I_e. The corresponding feedback transistor M_{ja} will drive this maximum current I_{oj} and be biased in saturation. Since the gate of transistors M_{1a}-M_{4a} is common and biased for the maximum current, this implies that for the nonmaximum branches transistors M_{ia} $(i \neq j)$ will be biased in ohmic region, thus producing a small drain-to-source voltage, which turns OFF the corresponding input transistors M_{ib}. Since the gate of M_{1a}-M_{4a} is set for the maximum input current, this current is copied by transistors M_5-M_7.

The MAX circuit composed of M_{1a}-M_{4a}, M_{1b}-M_{4b}, and I_e [20] works fine, except that it is slow. Note that the input currents I_{oi} can be positive and negative. This will cause large voltage excursions at the input nodes when the current changes from negative to maximum and back again, which will cause undesirable delays and limit the maximum possible frequency of the input sinusoids. To avoid this, NMOS transistors M_{1c}-M_{4c} have been introduced. These transistors should provide a very small negligible current when the corresponding input branch is driving the maximum, and provide a sufficiently high current for the other branches to avoid large voltage excursions. This is achieved by biasing the gate of the NMOS transistors M_{1c}-M_{4c} with the regulator circuit in Fig. 7(b). This circuit replicates one of the MAX circuit input branches (M_{fa} and M_{fb}), biased with a copy of current I_e and using an input current which is a copy of the maximum $I_{\rm env}$. Consequently, the voltages at the gates of M_{fa} and M_{fb} copy those of the branch with maximum input. A small fraction of the bias current εI_e is used to drive transistors M_{fc1} and M_{fc2}, while making their gate and source voltages equal. The gate voltage V_{rc} is used to bias the gate of transistor M_{1c}-M_{4c} in Fig. 7(a). The source voltage of M_{fc1} and M_{fc2} will be equal to that of M_{jc} of the maximum input branch. Consequently, this max branch M_{jc} transistor will drive current εI_e. For the other branches, since their M_{ic} transistor source voltage is lower, it will be injecting a higher current thus maintaining the node voltage sufficiently high to avoid set-on delays. The circuit was designed for $\varepsilon \approx 1/200$.

In order to minimize power consumption of the complete oscillator, the MAX circuit bias current I_e was made to depend linearly with the current that controls the oscillator frequency. More precisely, if I_A is the current controlling the differential pairs of OTA1 and OTA2 in Fig. 2 then, I_e in Fig. 7 was set to $I_e = I_A/5$. This way, for lower oscillating frequencies the MAX circuit is biased with less current since lower speed is required. On the other hand, for precise operation of the MAX circuit it is desirable to keep the four phases input signal amplitudes sufficiently high. For this purpose, the two extra outputs of OTA1 and OTA2 have a gain of 10 with respect to the original one, as we will see in the next Subsection. Consequently, if the oscillator amplitude control loop will set the amplitude to $I_A/5$ then the four inputs to the MAX circuit will have peak amplitudes of value 2 I_A. Therefore, in practice $I_{\rm ref}$ in Fig. 5 needs to be set to $I_{\rm ref} = 2I_A$.

Since the oscillation frequency is also a function of I_A, it results that both amplitude and frequency of the four phase inputs to the MAX circuit are determined by I_A (once the oscillator amplitude control loop has stabilized). To illustrate the proper operation of the MAX circuit we use the relationship between I_A and signal frequency obtained experimentally in Section VI and simulated the resulting average and ripple values for the output of the MAX circuit, while sweeping I_A. For an ideal four-phase MAX circuit, as shown in Fig. 4, the dc component of the output signal can be shown to be 90% of the input peak amplitude, while the ripple amplitude is 29%. Fig. 8 shows the simulated values for the average [Fig. 8(a)] and ripple [Fig. 8(b)] values in percentage as a function of I_A. Both stay reasonably close to the theoretical ideal values. Fig. 9 shows the simulated input and output current waveforms for four different values of I_A (and frequency): 1) $I_A = 7.0$ μA, $f = 50$ MHz; 2) $I_A = 16.0$ μA, $f = 80$ MHz; 3) $I_A = 26.0$ μA, $f = 105$ MHz; 4) $I_A = 37.0$ μA, $f = 130$ MHz.

B. Frequency Controlling OTAs

In the oscillator of Fig. 2(a), the frequency is set by the transconductance g_{mA} of OTA1 and OTA2, as given in (8). These OTAs need to provide a sufficiently high transconductance to produce the desired frequencies between 50 and 130 MHz, and at the same time, provide two extra current outputs of the opposite sign with ten times more current gain. The schematics of these OTAs are shown in Fig. 10. The circuit is based on a conventional differential pair OTA with cascode current mirrors [16]. The two extra outputs with current gain 10 are implemented by the cascade of current mirrors shown in Fig. 10(b). All PMOS transistors are of size $W/L = 6$ μm/0.8 μm and all NMOS transistors of size $W/L = 4$ μm/0.8 μm. This approach introduces a little extra load at nodes ν_a, ν_b, ν_c and ν_d in Fig. 10(a), thus deteriorating very slightly the frequency response of OTA1 and OTA2 (at

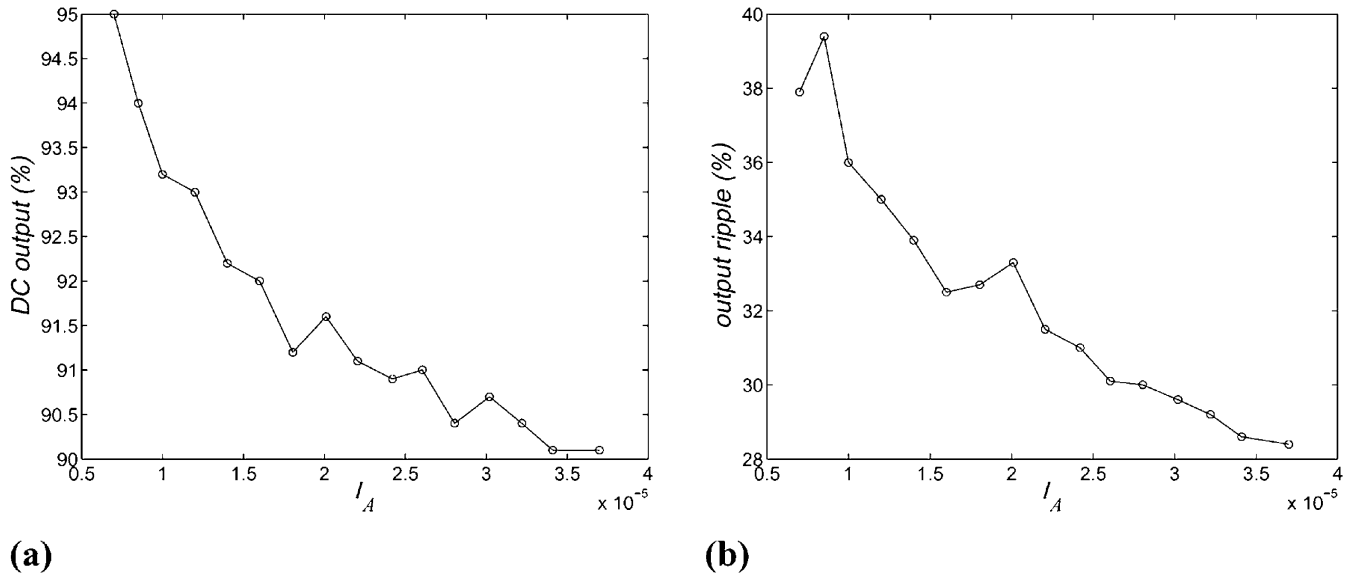


Fig. 8. Simulated performance of MAX circuit. (a) DC level of output in percent. (b) Ripple amplitude in percent.

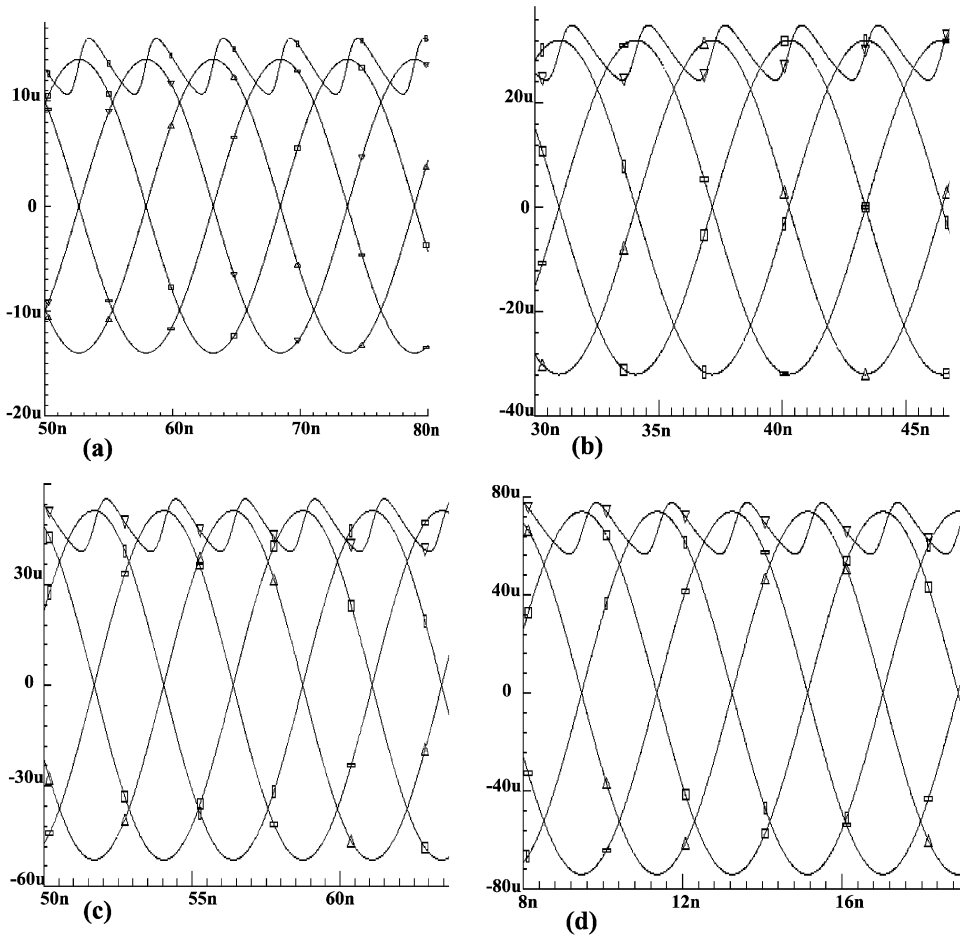


Fig. 9. Simulated input-output waveforms for the four-phase MAX circuit at different operating frequencies. (a) 50 MHz. (b) 80 MHz. (c) 105 MHz. (d) 130 MHz.

output I_o), while providing two high current gain outputs with tolerable extra delay. Note that the delay introduced by the cascade of mirrors in Fig. 10(b) does not affect the achievable oscillating frequency, because this frequency is limited by the frequency response of the OTAs at their nonamplifying output. On the other hand, a mismatch in the delays of the four amplifying outputs of OTA1 and OTA2 will cause the four phases in Fig. 4 to not be exactly at 90° phase difference. This will produce a higher ripple at the output of the MAX circuit, which is not very critical for the proper operation of

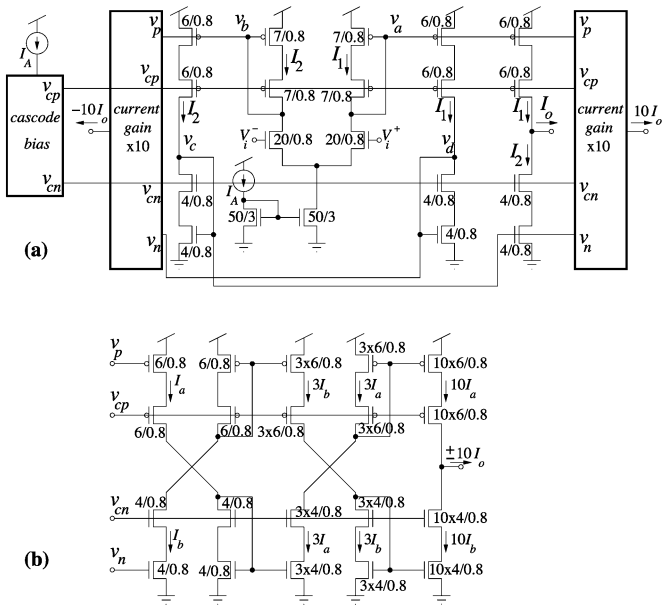


Fig. 10. (a) Circuit schematics for frequency controlling OTAs, (b) details of current amplifier circuit.

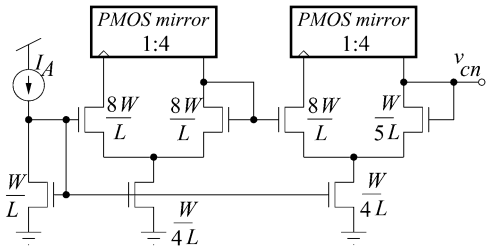


Fig. 11. Circuit used for providing NMOS cascode bias voltages.

the oscillator (remember we are assuming the ripple will be filtered out).

The cascode bias voltage ν_{cn} is obtained through the use of the circuit shown in Fig. 11 [21]. This circuit provides an appropriate cascode bias voltage whether transistors operate in strong, moderate or weak inversion. Its operation is based on the exploitation of the properties of transistor channel voltage at a relative distance from its source terminal, and a MOS transistor formulation valid in all modes of operation [22], [23]. The cascode voltage for the PMOS transistors ν_{cp} is obtained with a symmetrical version of the circuit shown in Fig. 11.

Simulation results for this OTA structure are shown in Fig. 12. Fig. 12(a) shows the obtained relationship between dc transconductance g_{mA} and bias current I_A, for all eight corner analysis simulation. The central thicker line corresponds to the "typical" corner. Fig. 12(b) shows the simulated values for the effective capacitance $C_A(f, I_A) = g_{mA}(I_A)/\omega_A(f, I_A)$ (see (7)). The surface $\omega_A(f, I_A)$ is computed from the simulated phase response $\phi_A(f, I_A)$ of the transconductance g_{mA} for different bias levels I_A. According to the transconductance model given in (1), ω_A and ϕ_A should be related by the following equation

$$\omega_A(f, I_A) = -\frac{2\pi f}{\tan(\phi_A(f, I_A))}. \tag{30}$$

As an illustration, Fig. 12(b) also shows the trajectory $C_A(f_{meas}(I_A), I_A)$, where the dependence $f_{meas}(I_A)$ has been obtained experimentally, as shown in Section VI. As can be seen, for this trajectory, the value of C_A stays fairly constant between 100 *fF* and 150 *fF*.

C. Amplitude Controlling OTAs

The amplitude control of oscillations is achieved by adjusting dynamically the transconductance of OTA3 and OTA4, as explained in Sections III and IV, and depicted in Fig. 5. For OTA3 and OTA4, the same OTA structure shown in Fig. 10(a) was used but without the extra current gain circuits.

Fig. 13 shows simulation results for the designed amplitude controlling OTA. The relationship between dc transconductance g_{mb} and bias current I_b is shown in Fig. 13(a) (for all eight corners), while the dependence of the effective capacitance C_b with operating frequency and bias current I_b is shown in Fig. 13(b). This surface has been computed from the simulated phase response of the OTA in the same way than explained previously for the frequency controlling OTA. During operation of the oscillator, there will be a trajectory in this surface as well, crossing it from the minimum to the maximum frequency. As can be seen, the value of C_b will not change much (in the worst case, it would change from 150 to 200 fF).

Note that for both effective capacitances C_A and C_b, their values do not change much (considering that frequency changes almost a factor of 3, I_b a factor of 3, and I_A almost a factor of 7). Consequently, for design purposes, one may assume that both C_A and C_b stay approximately constant, and use their values in (8) to predict frequency and transconductance ranges.

D. Simulations of Amplitude Control Loop

Extensive simulations were performed to validate the proper operation of the oscillator, specially the proposed amplitude control loop. In Section IV stability conditions were derived that resulted in mathematical relationships between parameters m, τ_{env}, $\tau_f = C_{cf}/g_{mf}$, ρ, and $\alpha i_{Ao}/2$. Parameter m, which is the ratio between the main envelope detector output and the two secondary outputs (see Fig. 5), is set to 1/5. Time constant τ_{env} is the time delay associated to the envelope detector. This delay can be characterized by simulating the envelope detector with an amplitude step in the four phases current inputs and observing the delay time constant at the output. This simulation needs to be performed sweeping the possible input frequency range, the input current amplitudes, and the corresponding bias current I_e. It was observed that the resulting time constant τ_{env} was always less than 5 *ns*. Regarding time constant $\tau_f = C_{cf}/g_{mf}$, the integrating capacitance C_{cf} (see Fig. 5) was set to 5 *pF*, and the transconductance of transistors M_{f1} and M_{f2} remained less than 100 μmhos over the whole operating range. Consequently, the minimum value for time constant τ_f was 50 *ns*. In what concerns the dc gain of the envelope detector ρ, from Fig. 8(a) we can see that it can change between 0.90 and 1.0. The most complicated parameter to estimate is $\alpha i_{Ao}/2$. From (23) and (27) we know that

$$\left|\frac{I_a(s)}{I_b(s)}\right| = \left|\frac{\alpha i_{Ao}}{2s}\right| \tag{31}$$

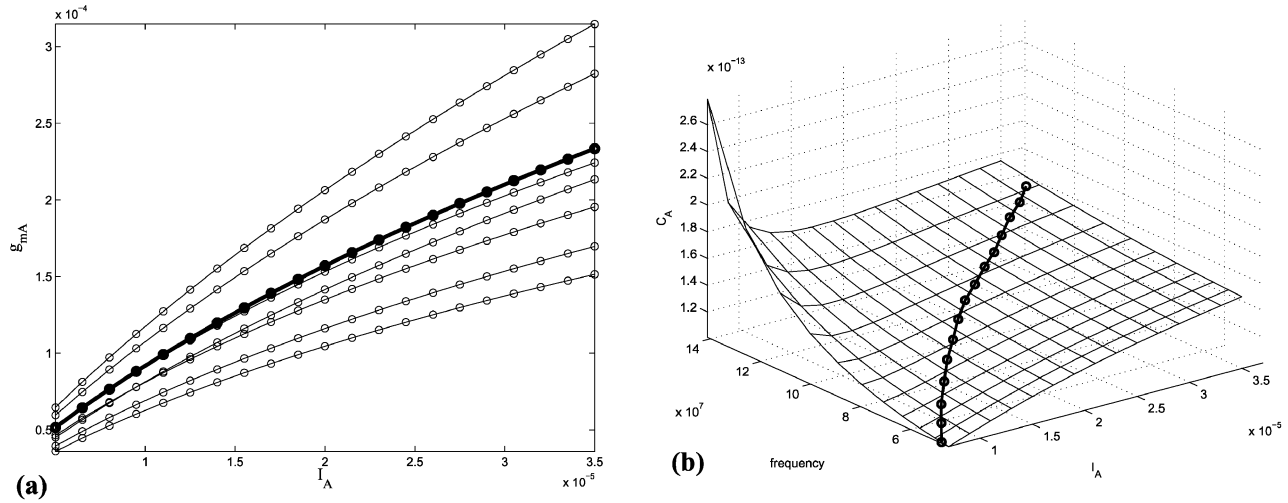


Fig. 12. Simulations for frequency controlling OTAs. (a) transconductance g_{mb} versus bias current I_A, (b) effective capacitance C_A versus bias current I_A and operating frequency.

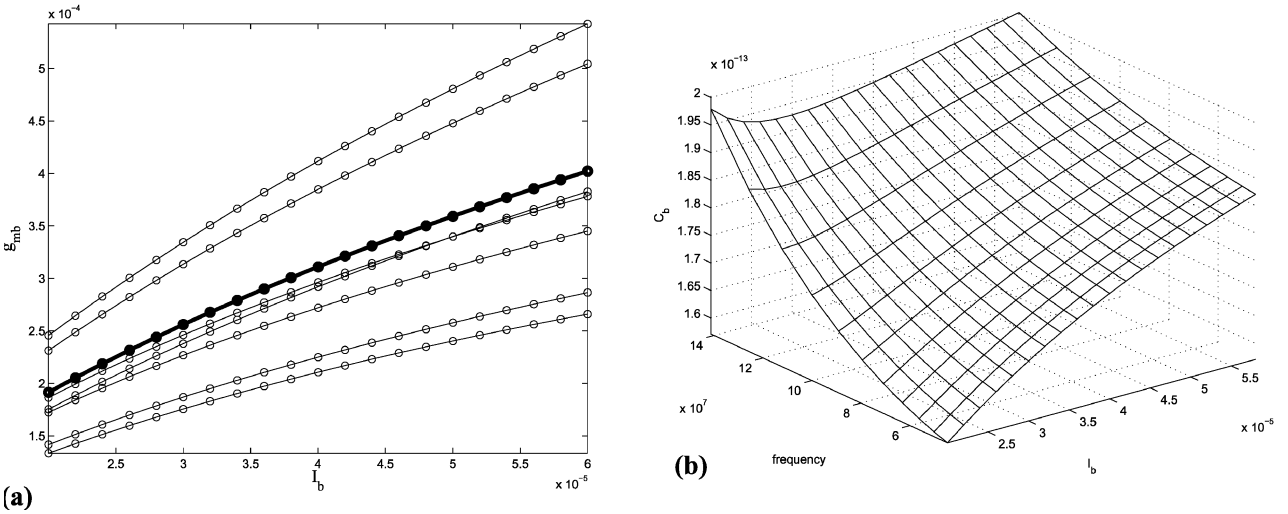


Fig. 13. Simulations for amplitude controlling OTAs. (a) transconductance g_{mb} versus bias current I_b, (b) effective capacitance C_b versus bias current I_b and operating frequency.

which defines the oscillator AC current amplitude $I_a(s)$ as the integral of the AC control current component $I_b(s)$, with integration time constant $2/(\alpha i_{Ao})$. The gain in (31) can be estimated by injecting a sinusoidal component in parallel with I_b in Fig. 5 and observing the modulated current amplitude at the output of OTAs g_{mA}. This is illustrated Fig. 14 where the oscillator is operating at 65 *MHz* with $I_b = 3.0\ \mu$A plus an added AC signal of 1 μA peak-to-peak amplitude and 1 *MHz* frequency (see lower trace in Fig. 14). As a result of this added AC component, the output current amplitude is modulated as shown in upper trace of Fig. 14. Note the $\pi/2$ phase shift between both signals, which is the result of one being the integral of the other as indicated in (31). In this particular case, the amplitude ratio between both AC signals in Fig. 14 is $|I_a/I_b| = 170\,\text{nA}/1\ \mu\text{A} = 0.17$, which according to (31) yields $\alpha i_{Ao}/2 = 2\pi \times 65\ \text{MHz} \times 0.17 = 69.4\ \text{MHz}$. Repeating similar simulations or the whole frequency range provides a variation interval for $\alpha i_{Ao}/2$ from 28 *MHz* to 150 *MHz*.

Using the worst case limits of all these parameters in the stability conditions of (29), results in

$$m > \frac{\tau_{\text{env}}}{\tau_f},\ \text{worst case}: \frac{1}{5} > \frac{5\ \text{ns}}{50\ \text{ns}} = \frac{1}{10}$$
$$m < \frac{2}{\alpha i_{Ao} \rho \tau_{\text{env}}},\ \text{worst case}: \frac{1}{5} < \frac{1}{150\ \text{MHz} \times 1.0 \times 5\ \text{ns}} = 1.35. \tag{32}$$

Figs. 15–17 illustrate the transient behavior of the AGC loop through some simulations. In Fig. 15 a step in current I_{ref} (see Fig. 5) was introduced to force the AGC loop to adjust to a new oscillating amplitude. The upper trace (a) is the oscillator voltage at one of the capacitors C, the middle trace (b) shows the evolution of the voltage at capacitor C_{cf}, and the lower trace (c) shows the step in reference current I_{ref}. Fig. 16 shows a simulation for which the value of parameter m was set to a very small value (1/50). As a result, the AGC loop turned out to be unstable. The figure shows the oscillator voltage amplitude at

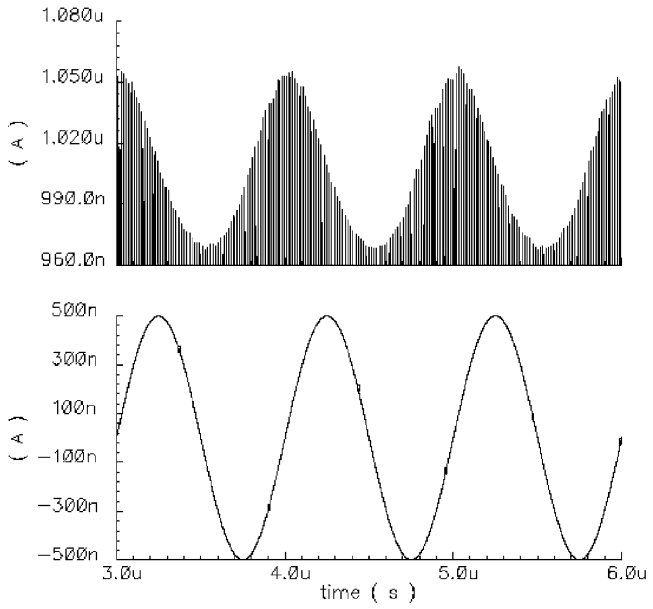


Fig. 14. Simulated relationship between $I_a(s)$ (upper trace) and $I_b(s)$ (lower trace).

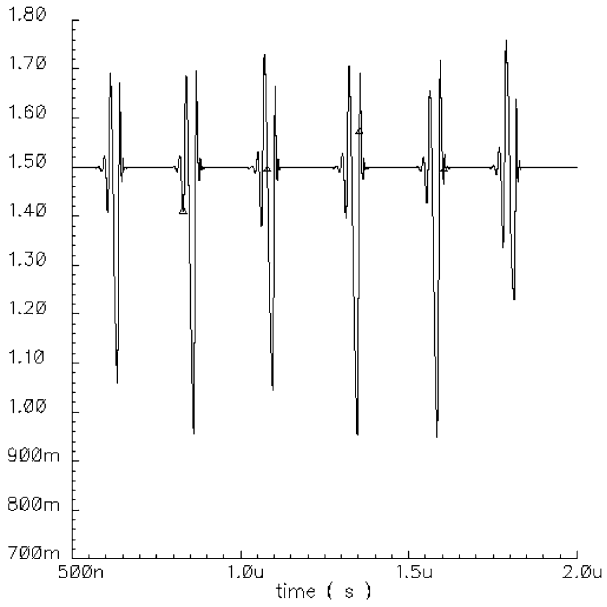


Fig. 16. Illustration of unstable AGC behavior when gain factor m is set to a very small value ($m = 1/50$).

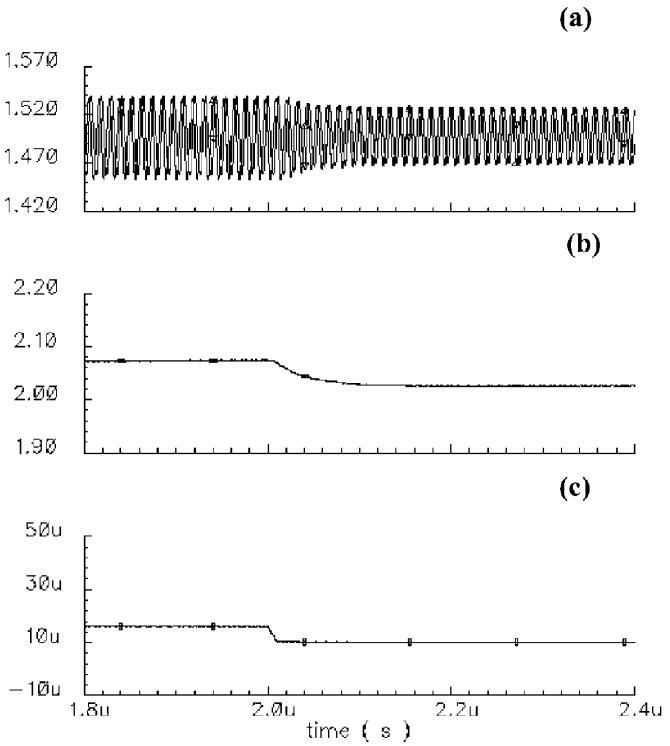


Fig. 15. Oscillator response to a step in the amplitude control signal $I_{\rm ref}$. (a) Oscillator voltage output, (b) voltage at node V_{cf}, (c) amplitude reference current $I_{\rm ref}$.

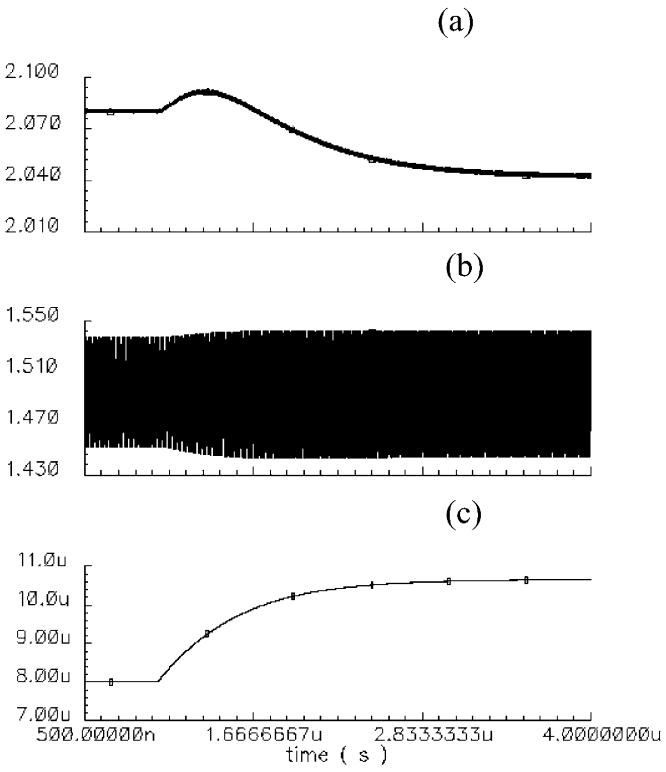


Fig. 17. Oscillator response to a step in the frequency control signal I_A. (a) voltage at node V_{cf}, (b) oscillator voltage output, (c) current I_A.

one of the capacitors C. Fig. 17 shows a simulation where a step in the frequency controlling current I_A was introduced. The upper trace (a) shows the evolution of voltage V_{cf} (see Fig. 5), the middle trace (b) shows the oscillator output voltage at one of the C capacitors, and the lower trace shows a scaled replica (1/5) of control current I_A.

VI. Experimental Results

A complete oscillator prototype was fabricated in the AMS 0.8-μm CMOS process. The oscillator used an active area of 0.20 mm^2. Most of it (0.15 mm^2) was used by the cascade of current mirrors within the frequency controlling OTAs. Fig. 18 shows a microphotograph of the oscillator, indicating the main

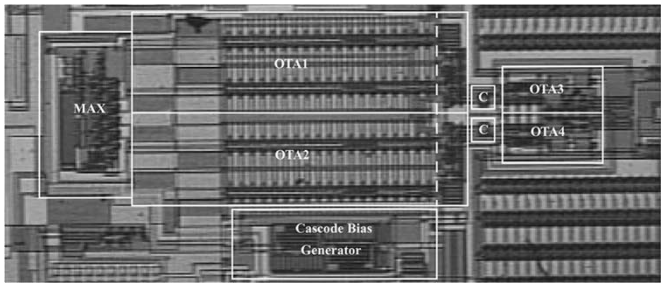


Fig. 18. Chip microphotograph containing the complete quadrature oscillator.

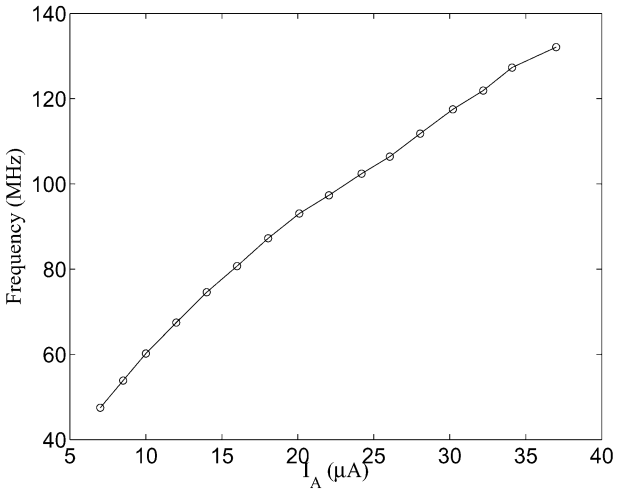


Fig. 19. Measured relationship between oscillation frequencies and bias current I_A.

building blocks. For OTA1 and OTA2 the dashed line separates the current amplifying cascade of mirrors (larger area) from the rest of the OTA (smaller area).

The frequency was tunable between 48 MHz to 132 MHz, through the OTA1 and OTA2 transconductance bias current I_A. The dependence between the measured oscillation frequency and bias current I_A is shown in Fig. 19.

The oscillations at nodes V_1 and V_2 (see Fig. 2) were monitored by two voltage buffers and driven off-chip to verify their phase shift as a function of frequency. Fig. 20 shows the measured phase difference between both signals, in degrees, versus the frequency of oscillation.

The cause of quadrature phase error is mismatch between transconductances and capacitances. Note that perfect symmetry in the oscillator yields perfect quadrature phase shift. Consequently, any source of asymmetry will increase phase error between the two quadrature components. We had available a very reduced number of samples, all of which produced similar results. However, in order to have a statistical estimate of the phase error, we performed Monte Carlo simulations based on mismatch parameters provided by the manufacturer. Those simulations yielded phase errors of standard deviation around 2°. Appendix B includes a mathematical analysis that estimates phase error based on component mismatch. Monte Carlo simulations of the different oscillator components reveals that the main source of phase error is the mismatch in

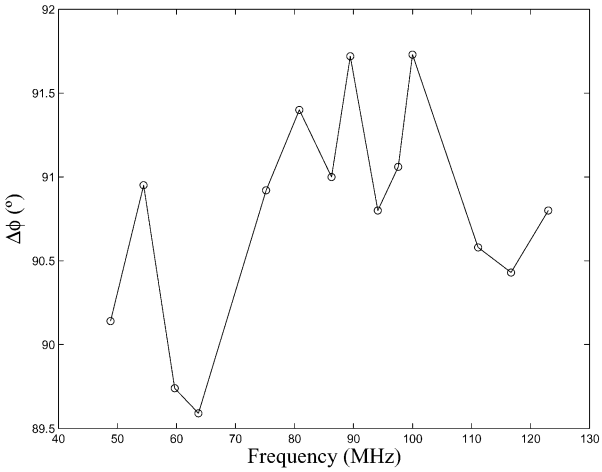


Fig. 20. Measured phase difference between voltages V_1 and V_2 of the quadrature oscillator, as a function of oscillation frequency.

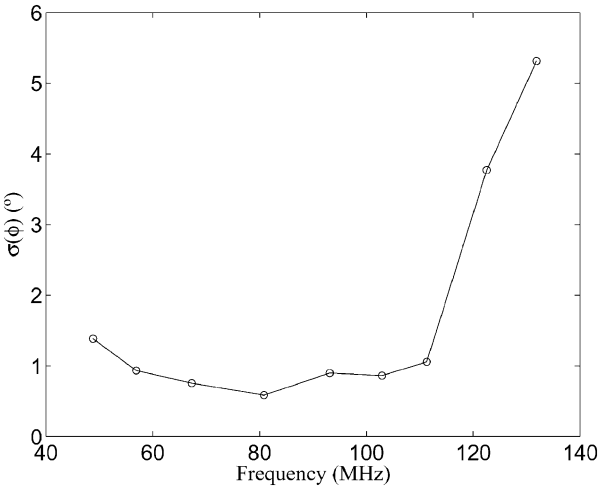


Fig. 21. Measured phase noise as a function of frequency, expressed as the standard deviation of the zero crossings in degrees.

transconductance of the OTAs. For the transistor sizes used in the design, the standard deviation of the transconductances was around 9%. Using this value in (43) and (46) of Appendix B (and neglecting capacitances mismatch, which was below 1%) results in phase error with standard deviation $\sigma(\Delta\phi) \approx 1.8°$ ($\sigma(\Delta\delta_{\text{img}}) \approx 6.4\%$ rad).[2].

The oscillator operates at small amplitudes (less than 100 mV). For such amplitudes, phase noise contribution cannot be neglected. In order to estimate the phase noise, the voltage waveforms were recorded for several hundreds of cycles at 0.2-ns sampling rate. The zero crossings were computed by performing linear interpolations on the two consecutive samples before and after a transition from negative to positive (or from positive to negative). The phase noise is obtained by computing the standard deviation on these zero crossings, expressed in degrees. The result is shown in Fig. 21, as a function of oscillation frequency.

[2]In our simulations, we observed that if mismatch is relatively high the AGC could loose track and amplitude would be controlled by elements nonlinearities [18], resulting in larger amplitudes and much higher distortions.

VII. Conclusion

An OTA-C topology for implementing a quadrature oscillator in the range 50–130 MHz has been presented. The topology exploits symmetry to produce the two phases at 90° phase shift. The circuit also produces four extra current signals at phases 0°, 90°, 180°, 270°, which are used in a high-speed current-mode MAX circuit to extract a quasi-instantaneous envelope of the oscillations, in the current domain. This envelope is used in a properly stabilized amplitude control loop to set the oscillating amplitude at 1/5 of the current excursion range of the main OTAs, to minimize distortion. The influence of transconductance phase shift of the OTAs is considered and properly modeled and estimated in the design. A complete oscillator prototype has been fabricated and tested in the AMS 0.8-μm CMOS process.

Phase noise has also been characterized. Appendix C analyzes the impact of quadrature phase error on the performance of the impedance probe mentioned in the introduction. Ironically, for such specific application, the system is not sensitive to phase error nor phase noise.

The fabricated prototype does not include a frequency tuning loop for making its frequency independent of temperature and process variations. Such tuning loops have been developed in the past for voltage controlled oscillators [13] and can be directly included in the present prototype.

Appendix A

For the amplitude control loop described in Sections III and IV, the speed of the amplitude control loop can be optimized by adjusting the poles of (28)

$$s_o = -\frac{k_2}{2k_1} \pm j\frac{\sqrt{4k_1 - k_2^2}}{2k_1} \tag{33}$$

where we assume

$$4k_1 - k_2^2 \geq 0 \Leftrightarrow \frac{8\tau_f}{\alpha\rho i_{A_o}} \geq (m\tau_f + \tau_{\rm env})^2. \tag{34}$$

To maximize speed, we need to make the real part of s_o as large as possible

$$\frac{k_2}{2k_1} = \frac{1}{2}\frac{m\tau_f - \tau_{\rm env}}{\frac{2\tau_f}{\alpha\rho i_{A_o}} - m\tau_f\tau_{\rm env}}. \tag{35}$$

For example, we can make the denominator zero (or $+\varepsilon$) for the maximum required amplitude $i_{A_{\max}}$. This would yield[3] [See (29)]

$$m = \frac{2}{\alpha\rho\tau_{\rm env} i_{A_{\max}}}. \tag{36}$$

Under this constraint, (35) becomes

$$\frac{k_2}{2k_1} = \frac{1}{2}\frac{\tau_{\rm env}^{-1} - \frac{\alpha\rho}{2} i_{A_{\max}}\tau_{\rm env}\tau_f^{-1}}{\frac{i_{A_{\max}}}{i_{A_o}} - 1}. \tag{37}$$

[3]Of course, this is an upper bound that should never be reached because otherwise s_o in (33) may end up with a positive real part, and consequently producing an unstable system. To play safe, just consider $i_{A_{\max}}$ to be larger than the maximum possible value.

Maximizing the numerator implies the condition

$$\tau_f \gg \frac{\alpha\rho}{2} i_{A_{\max}}\tau_{\rm env}^2 \tag{38}$$

which will make the final pole real part equal to $\mathrm{Real(s_o)} = -\mathrm{k_2/(2k_1)} \approx -\mathrm{i_{A_o}/(2i_{A_{max}}\tau_{env})}$. Here, we also have assumed the worst case $i_{A_{\max}} \gg i_{A_o} = i_{A_{\min}}$. For critically damped transient response one can further adjust the Q factor of the poles $\xi = 1/(2Q) = k_2/(2\sqrt{k_1}) = 1/(\sqrt{2})$, which means that $\tau_f = \alpha\rho i_{A_{\max}}\tau_{\rm env}^2(0.5 + i_{A_{\max}}/i_{A_o})$. If this is adjusted for $i_{A_{\min}} \ll i_{A_{\max}}$, then $\tau_f \approx (\alpha\rho\tau_{\rm env}^2 i_{A_{\max}})^2/i_{A_{\min}}$. This, together with (36), yields

$$m\tau_f = 2\tau_{\rm env}\frac{i_{A_{\max}}}{i_{A_{\min}}}. \tag{39}$$

The designer will usually try to make $\tau_{\rm env}$ as small as possible (fast envelope detection). The values for $i_{A_{max}}$ and $i_{A_{min}}$ are usually given. Since the designer has more control on parameters m and τ_f, these two can be made to satisfy the constraint in (39) for optimum critically damped transient response, while maintaining the conditions in (29), (34), (36) and (38).

Also, keep in mind that all this analysis is based on a set of assumptions and approximations (for example, modeling delays with zeros) which renders the resulting expressions and conditions as approximate. They will not be satisfied exactly. However, they turn out to be very helpful during the design process guiding the choice of parameters.

Appendix B

For mismatch analysis, let us use parameters g_{mAi}, g_{mbi}, C_i, $C_{Ai} = g_{mAi}/\omega_{Ai}$, and C_{bi}/ω_{bi} $(i = 1, 2)$, instead of without subscript i as used in Section II. Then, the mismatch parameters under consideration will be $\Delta C = C_2 - C_1$, $\Delta C_A = C_{A2} - C_{A1}$, $\Delta C_b = C_{b2} - C_{b1}$, $\Delta g_{mA} = g_{mA2} - g_{mA1}$, and $\Delta g_{mb} = g_{mb2} - g_{mb1}$. The relationship between voltages $V_1(s)$ and $V_2(s)$ will be now

$$\left(\frac{V_1}{V_2}\right)^2 = -\frac{sC_2 - sC_{b2} + g_{mb2}}{sC_1 - sC_{b1} + g_{mb1}}\frac{g_{mA2} - sC_{A2}}{g_{mA1} - sC_{A1}} \tag{40}$$

instead of (5) in Section II. Using (8) in (40) and assuming relatively small mismatch results in

$$\left(\frac{V_1}{V_2}\right)^2 \approx -1 + \delta_{\rm real} + j\delta_{\rm img} \tag{41}$$

where

$$\delta_{\rm img} \approx -\frac{\frac{C_A}{C-C_b}}{1 + \left(\frac{C_A}{C-C_b}\right)^2} \times \left[\frac{\Delta C - \Delta C_b}{C - C_b} - \frac{\Delta C_A}{C_A} - \frac{\Delta g_{mb}}{g_{mb}} + \frac{\Delta g_{mA}}{g_{mA}}\right]. \tag{42}$$

The first coefficient is always less or equal than 0.5. Consequently, the standard deviation of δ_{img} will be such that

$$\sigma^2(\delta_{\text{img}}) \leq \frac{1}{4}\left[\frac{\sigma^2(\Delta C)+\sigma^2(\Delta C_b)}{(C-C_b)^2} + \sigma^2\left(\frac{\Delta C_A}{C_A}\right)+\sigma^2\left(\frac{\Delta g_{mb}}{g_{mb}}\right)+\sigma^2\left(\frac{\Delta g_{mA}}{g_{mA}}\right)\right]. \tag{43}$$

Since δ_{real} and δ_{img} in (41) are much less than unity, then

$$\frac{V_1}{V_2} \approx \frac{\delta_{\text{img}}}{2} + j\left(1-\frac{\delta_{\text{real}}}{2}\right) \tag{44}$$

and the phase $\alpha = \pi/2 - \Delta\phi$ between V_1 and V_2 at the steady state will be

$$\tan(\alpha) = \frac{1-\frac{\delta_{\text{real}}}{2}}{\frac{\delta_{\text{img}}}{2}} \tag{45}$$

or equivalently, for small δ_{img} and δ_{real}

$$\Delta\phi \approx \frac{\frac{\delta_{\text{img}}}{2}}{1-\frac{\delta_{\text{real}}}{2}} \approx \frac{\delta_{\text{img}}}{2}. \tag{46}$$

APPENDIX C

Let us analyze, for the impedance bridge in Fig. 1, the effect of having an oscillator producing two signals that are not in quadrature. Let us assume both oscillator outputs have a generic phase difference of value ϕ. Signals $V_1(t)$ and $V_2(t)$ are sinusoidal and of the same frequency ω than the oscillator

$$\begin{aligned} V_1(t) &= a\cos(\omega t+\alpha) \\ V_2(t) &= b\cos(\omega t+\beta). \end{aligned} \tag{47}$$

If the impedances in the bridge are identical in the two branches, then both amplitudes and phases will be equal. Otherwise, amplitudes and phases will not be equal. The error signals produced by the system are

$$\begin{aligned} e_1(t) &= [a\cos(\omega t+\alpha) - b(\cos(\omega t+\beta)]\cos(\omega t) \\ &= \frac{a}{2}\cos(2\omega t+\alpha) - \frac{b}{2}\cos(2\omega t+\beta) + \frac{a}{2}\cos\alpha - \frac{b}{2}\cos\beta \\ e_2(t) &= [a\cos(\omega t+\alpha) - b\cos(\omega t+\beta]\cos(\omega t+\phi) \\ &= \frac{a}{2}\cos(2\omega t+\alpha+\phi) - \frac{b}{2}\cos(2\omega t+\beta+\phi) \\ &\quad + \frac{a}{2}\cos(\alpha-\phi) - \frac{b}{2}\cos(\beta-\phi). \end{aligned} \tag{48}$$

After low-pass filtering both error signals, their dc components are

$$\begin{aligned} e_{1,dc} &= \frac{a}{2}\cos(\alpha) - \frac{b}{2}\cos(\beta) \\ e_{2,dc} &= \frac{a}{2}\cos(\alpha-\phi) - \frac{b}{2}\cos(\beta-\phi). \end{aligned} \tag{49}$$

The closed control loop in Fig. 1 will make both low-pass filtered error signals equal to zero, thus solving

$$\begin{aligned} a\cos\alpha &= b\cos\beta \\ (a\cos\alpha - b\cos\beta)\cos\phi &= -(a\sin\alpha - b\sin\beta)\sin\phi \end{aligned} \tag{50}$$

which is equivalent to solving

$$\begin{aligned} a\cos\alpha &= b\cos\beta \\ a\sin\alpha &= b\sin\beta \end{aligned} \tag{51}$$

whose solution is $a = b$ and $\alpha = \beta$. Consequently, if the signal-processing block and control loop are stable, then in the steady state both voltages $V_1(t)$ and $V_2(t)$ will be identical, independently of the specific value of ϕ, as long as it is nonzero. Therefore, for the specific system in Fig. 1 it is not necessary to have a quadrature oscillator with very little phase error.

Regarding the influence of noise, note that the system operates using the dc components of the error signals. Since noise is not folded into the dc level of the error signals, the system is also insensitive to noise in the oscillator.

REFERENCES

[1] W. R. Scott and G. S. Smith, "Measured electrical constitutive parameters of soil as functions of frequency and moisture-content," *IEEE Trans. Geosci. Remote Sensing*, vol. 30, pp. 621–623, May 1992.

[2] W. S. Rial and Y. J. Han, "Assessing soil water content using complex permittivity," *Trans. ASAE*, vol. 43, no. 6, pp. 1979–1985, 2000.

[3] J. O. Curtis, "A durable laboratory apparatus for the measurement of soil dielectric properties," *IEEE Transa. Instrum. Meas.*, vol. 50, pp. 1364–1369, Oct. 2001.

[4] S. V. Pezzi, "Device for the simultaneous determination of humidity and conductivity in soils or low dielectric constant material," Spain Patent 2 111 444.

[5] S. Smith, *Microelectronic Circuits*, 4th ed. New York: Oxford Univ. Press, 1998.

[6] P. P. Bey, D. J. Yonce, and T. L. Fare, "Stability analysis of an autonulling AC bridge for use with silicon-based sensors," *IEEE Trans. Circuits Syst. I*, vol. 41, pp. 210–219, Mar. 1994.

[7] R. L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits Device Mag.*, vol. 1, pp. 20–32, Mar. 1985.

[8] E. Sánchez-Sinencio and J. Silva-Martínez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," *Proc. Inst. Elect. Eng. G, Circuits, Dev., Syst.*, vol. 147, pp. 3–12, Feb. 2000.

[9] Y. Tsividis and J. O. Voorman, Eds., *Integrated Continuous-Time Filters: Principles, Design and Applications*. New York: IEEE Press, 1992.

[10] P. M. VanPeteghem and R. Song, "Tuning strategies in high-frequency integrated continuous-time filters," *IEEE Trans. Circuits Syst.*, vol. 36, pp. 136–139, Jan. 1989.

[11] C. Plett and M. A. Copeland, "A study of tuning for continuous-time filters using macromodels," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 524–531, Aug. 1992.

[12] S. Lindfors, K. Halonen, and M. Ismail, "A 2.7 V elliptical MOSFET-only g_m C-OTA filter," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 89–95, Feb. 2000.

[13] B. Linares-Barranco, A. Rodríguez-Vázquez, J. L. Huertas, and E. Sánchez-Sinencio, "On the generation design and tuning of OTA-C high-frequency sinusoidal oscillators," *Proc. Inst. Elect. Eng. G, Circuits, Dev., Syst.*, vol. 139, no. 5, pp. 557–568, 1992.

[14] A. Rodríguez-Vázquez, B. Linares-Barranco, J. L. Huertas, and E. Sánchez-Sinencio, "On the design of voltage controlled sinusoidal oscillators using OTAS," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 198–211, Feb. 1990.

[15] A. Buonomo, C. D. Bello, and O. Greco, "On the existence and uniqueness of stable quasi-sinusoidal oscillations," *Proc. Int. J. Circuit Theory Applicat.*, vol. 13, pp. 327–335, 1985.
[16] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. New York: Oxford Univ. Press, 2002.
[17] B. Linares-Barranco and T. Serrano-Gotarredona, "A loss control feedback loop for VCO stable amplitude tuning of RF integrated filters," in *Proc. 2002 IEEE Int. Symp. Circuits and Systems (ISCAS'02)*, vol. 1, May 2002, pp. 521–524.
[18] B. Linares-Barranco and A. Rodríguez-Vázquez, "Harmonic oscillators," in *Encyclopedia of Electrical and Electronics Engineering*, J. G. Webster, Ed. New York: Wiley, 1999, vol. 8, pp. 632–642.
[19] E. Vannerson and K. C. Smith, "Fast amplitude stabilization of an RC oscillator," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 176–179, Aug. 1974.
[20] J. Lazzaro, R. Ryckebush, M. A. Mahowald, and C. A. Mead, "Winner-take-all networks of O(N) complexity," *Adv. Neur. Inf. Processing Syst.*, vol. 1, pp. 703–711, 1989.
[21] P. Heim and M. A. Jabri, "MOS cascode-mirror biasing circuit operating at any current level with minimal output saturation voltage," *Electron. Lett.*, vol. 31, no. 9, pp. 690–691, 1995.
[22] C. C. Enz, F. Krummernacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Anal. Integr. Circuits Signal Processing J.*, vol. 8, pp. 83–114, 1995.
[23] C. Galup-Montoro, M. C. Schneider, and A. I. A. Cunha, "A current-based MOSFET model for integrated circuit design," in *Low-Voltage/Low-Power Integrated Circuits and Systems*, E. Sánchez-Sinencio and A. G. Andreou, Eds. New York: IEEE Press, 1998, ch. 2.

Bernabé Linares-Barranco received the B.S. degree in electronic physics, the M.S. degree in microelectronics, and the Ph.D. degree in high-frequency operational transconductance amplifiers oscillator design from the University of Seville, Seville, Spain, in 1986, 1987, and 1990, respectively, and the Ph.D degree in analog neural network design from Texas AM University, College Station, in 1991.

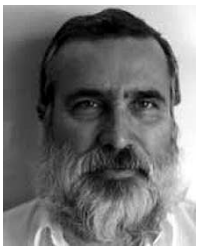
From 1991 to 2003, he was a Tenured Scientist at the Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain, where, in 2003, he was promoted to Tenured Researcher, and in 2004, to Full Professor. From September 1996 to August 1997, he was a Postdoctoral Fellow on sabbatical in the Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD. During Spring 2002, he was a Visiting Associate Professor in the Electrical Engineering Department, Texas A&M University, College Station. He has been involved with circuit design for telecommunication circuits, very large-scale integration (VLSI) emulators of biological neurons, VLSI neural-based pattern-recognition systems, hearing aids, precision circuit design for instrumentation equipment, bio-inspired VLSI vision processing systems, transistor parameters mismatch characterization, address-event-representation VLSI, RF circuit design, and real-time vision-processing chips. He is coauthor of the book *Adaptive Resonance Theory Microchips* (Norwell, MA: Kluwer, 1998).

Dr. Linares-Barranco was corecipient of the 1997 IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION SYSTEMS Best Paper Award for the paper, "A Real-Time Clustering Microchip Neural Engine," and of the 2000 IEEE CAS Darlington Award for the paper "A General Translinear Principle for Subthreshold MOS Transistors." He organized the 1994 Nips Post-Conference Workshop "Neural Hardware Engineering." From July 1997 until July 1999, he was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, and since January 1998, is an Associate Editor of the IEEE TRANSACTIONS ON NEURAL NETWORKS and was its Chief Guest Editor for the Special Issue on Neural Hardware Implementations.

Teresa Serrano-Gotarredona received the B.S. degree in electronic physics and the Ph.D degree in very large-scale integration (VLSI) neural categorizers from from the University of Seville, Seville, Spain, after completing all her research at Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain, in 1992 and 1996, respectively, and the M.S. degree in electrical and computer engineering from the Johns Hopkins University, Baltimore, MD, (where she was sponsored by a Fulbright Fellowship), in 1997.

She was on a sabbatical stay in the Electrical Engineering Department,Texas A&M University, College Station, during Spring 2002. She was an Assistant Professor at the University of Seville from 1998 until 2000. Since June 2000, she is a Tenured Scientist at IMSE. Her research interests include analog circuit design of linear and nonlinear circuits, VLSI neural-based pattern-recognition systems, VLSI implementations of neural computing and sensory systems, transistor parameters mismatch characterization, address-event-representation VLSI, RF circuit design, and real-time vision processing chips. She is coauthor of the book *Adaptive Resonance Theory Microchips* (Norwell, MA: Kluwer, 1998).

Dr. Serrano-Gotarredona was corecipient of the 1997 IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION SYSTEMS Best Paper Award for the paper, "A Real-Time Clustering Microchip Neural Engine," and of the IEEE CAS Darlington Award for the paper "A General Translinear Principle for Subthreshold MOS Transistors."



Juan Ramos-Martos received the Licenciado degree in physics and the M.Sc. degree in electronics engineering from the University of Seville, Seville, Spain, and the Philips Institute of Technological Studies, Eindhoven, The Netherlands, in 1973 and 1976, respectively.

After working with two electronic companies start-ups (one in Spain, and the other in Switzerland), he joined Compañía Sevillana de Electricidad, first as Operations and Maintenance Director of the Small Solar Power System, an experimental solar power station, Tabernas, Spain, and later at the company's engineering department, Seville, Spain, participating in the deployment of a new Energy Management System and in Control and Telemetry applications. In 1991, he joined the Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain, as the Manager of industrial relations while also performing research work on microsensors interfacing. He has participated in several European projects in that field. He has also been executive manager for the dissemination activities of the mixed- signal design cluster of the European Commission. His current interests are in mixed-signal analog integrated circuits for industrial applications and interface circuits for inertial capacitive microsensors.

Joaquín Ceballos-Cáceres received the B.S. degree in electronic physics and the M.S. degree in microelectronics, from the University of Seville, Seville, Spain, in 1993 and 1999, respectively.

Since April 1996, he is a Member of the Technical Staff at the Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain, where he is currently an Assistant Manager of the Research and Development section. His main areas of interest include the design and testing of analog and mixed integrated circuits. He has been in the design teams of different research projects dealing with integrated circuits and systems.

José Miguel Mora received the BSc. degree and the M.Sc. degree in telecommunication engineering, specializing in microelectronics, from the Technical University of Madrid, Madrid, Spain, in 1990 and 1992, respectively.

Since April 1992, he is a Member of the Technical Staff at the Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain, where he is currently an Assistant Manager of the Research and Development section. His main areas of interest include the design and testing digital and mixed integrated circuits and field-programmable gate arrays, design of test structures for multichip modules. He has been in the design teams of different research projects dealing with integrated circuits and systems.

Alejandro Linares-Barranco received the B.S. degree in computer engineering, the M.S. degree in industrial computer science, and the Ph.D. degree in computer science (specializing in computer interfaces for bioinspired systems) from the University of Seville, Seville, Spain, in 1998, 2002, and 2003, respectively.

From January 1998 to June 1998, he was Second Lieutenant in the Spanish Airforce working as system administrator and software developer. During 1998, he also worked at the Colors Digital Communications S.L. Company, Seville, Spain. From November 1998 to February 2000, he was a Member of the Technical Staff at the Seville Microelectronics Institute (IMSE), an institute of the National Microelectronics Center (CNM), Spanish Research Council (CSIC), Seville, Spain. From March 2000 to February 2001, he was a Development Engineer in the Research and Development Department, SAINCO company, Seville, Spain, working on VHDL-based field programmable gate array (FPGA) systems for the INSONET European project on power line communications. Since March 2003, he is an Assistant Professor of Computer Architecture and Technology at the University of Seville. His research interests include VLSI and FPGA digital design, vision processing systems, bus emulation, and computer architectures.