iCaveats –a Project on the Integration of Architectures and Components for Embedded Vision

iCaveats
Integration of components and architectures for embedded vision

IMSE-cnm Instituto de Microelectrónica de Sevilla
R. Carmona-Galán
J. Fernández-Berni
A. Rodríguez-Vázquez

CiTIUS Centro Singular de Investigación en Tecnoloxías da Información
P. López
V. Brea
D. Cabello

Universidad Politécnica de Cartagena
G. Domenech-Asensi
R. Ruiz-Merino
J. Zapata-Pérez

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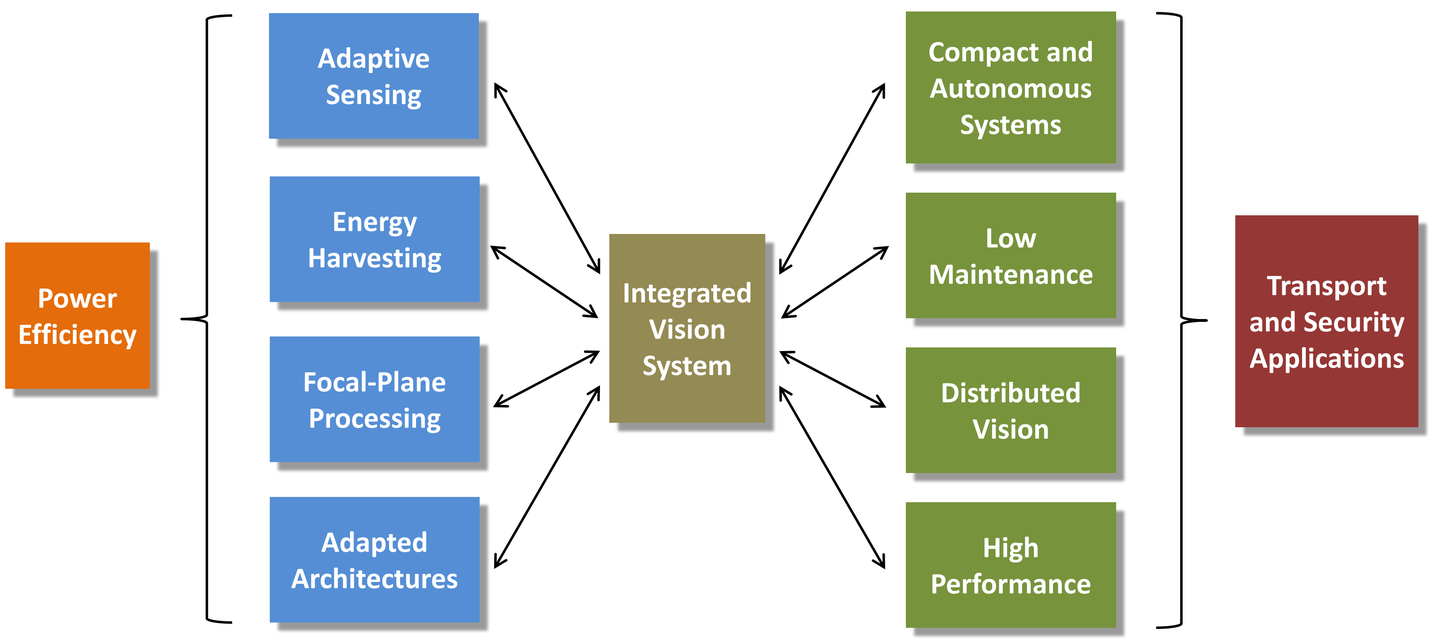
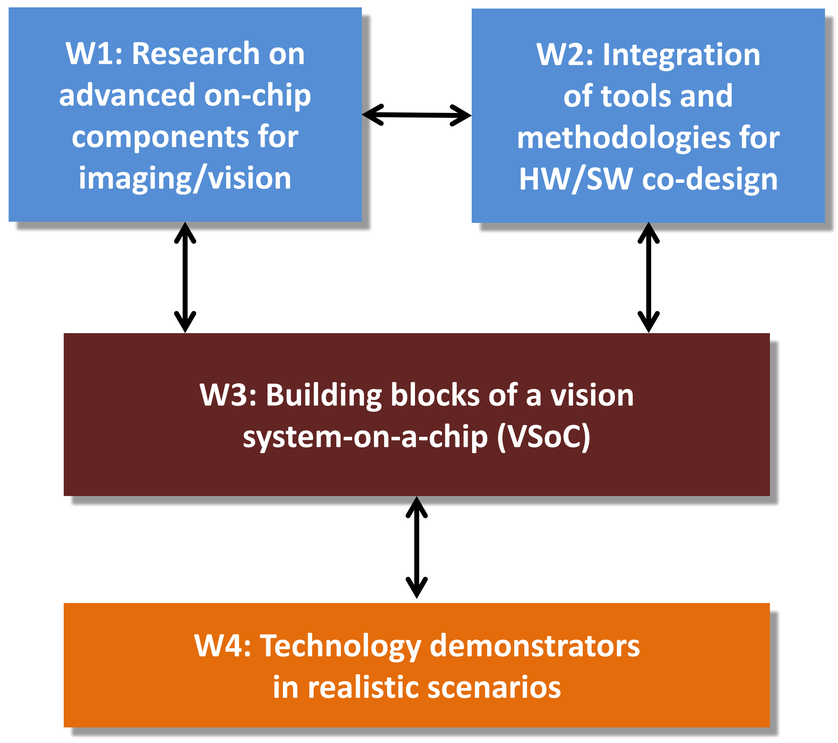
Abstract

The visual stimulus contains a great deal of data, demanding a considerable computational effort to be processed and interpreted. Compact and low-power implementation of an autonomous vision system is not easy to accomplish. Efficiency can be achieved by distributed resources and relatively coarse mixed-signal processing blocks. The main problem of this approach is the lack of flexibility to be migrated to other application fields. The objective of project **iCaveats** is developing a library of hardware components and architectures that would be transparent to the application developer. We have worked in hardware acceleration of image processing tasks, new sensor capabilities, energy management and sensory chip interfacing.

Initial hypothesis



PERT diagram

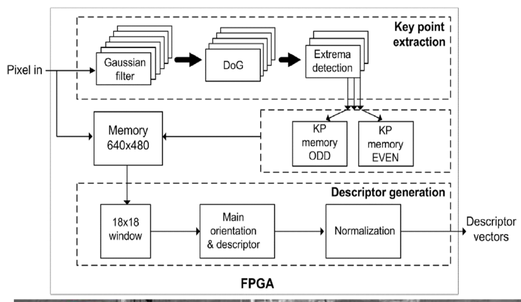


Project results

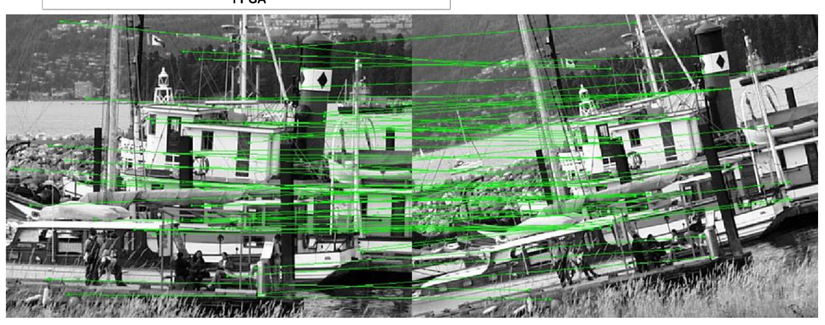
HW-Oriented Pixel-Based Adaptive Segmenter

- Evaluation of hardware non-idealities
- In-sensor foreground segmentation

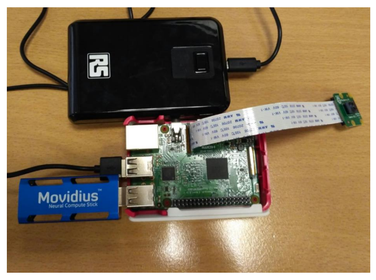
All-hardware SIFT implementation



- Virtex 5
- 3072 KPs @99fps
- 12k reg. + 14k LUTs
- 8.2 MB RAM
- 150 DSPs
- 100 MHz clock

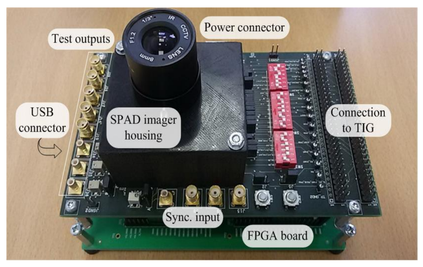


Real-time DNN inference in Raspberry-Pi



- Neural Computing Stick
- Caffe
- SqueezeNet
- 58.6 ms/frame
- 17.16 fps
- 3.07-3.90 W
- 2.83 matches/J (top-1)

SPAD camera prototype

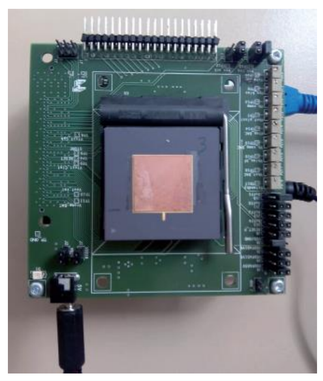


- 64× 64px SPAD imager
- PDE 5% @640nm
- 1.1 kfps
- Resolution 1cm
- Min. illumination 160uW
- XEM3010 FPGA board

Tracking by detection on Jetson TX2

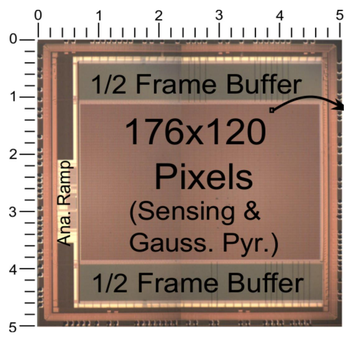
- NVIDIA embedded computer for AI
- HO-PBAS + GOTURN
- Adapted for multiple object detection and tracking

Sun sensor for satellite navigation



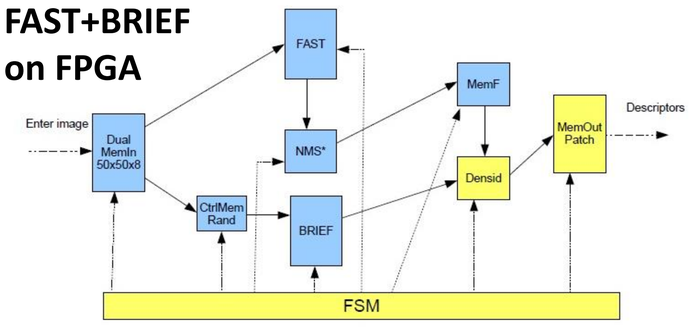
- Reduced data flow
- Latency < 5ms
- Dynamic range > 100dB
- Resolution 0.03°
- Accuracy
  - 0.0132° (θ)
  - 0.05° (ϕ)

Gaussian Pyramid CMOS vision sensor



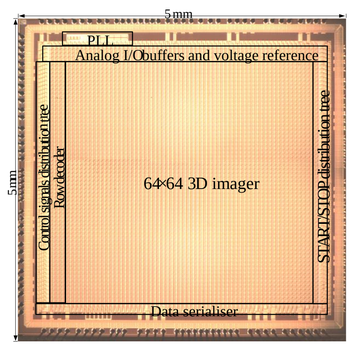
- 0.18µm CMOS technology
- Power: 70mW
- Frame rate: 125 fps
- 26.5 nJ/px @ 2.64 Mpx/s
- 3D-integrable architecture

FAST+BRIEF on FPGA

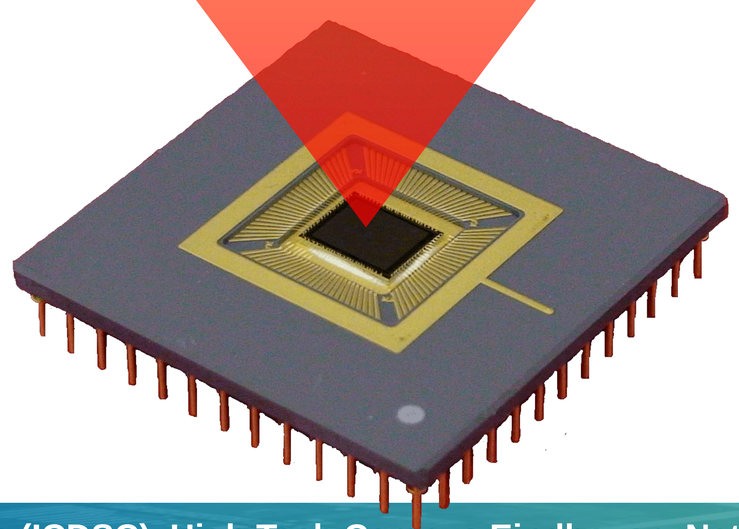


- Gaussian kernel for BRIEF
- Ethernet and lwIP for image data transmission
- Descriptor + corner detector

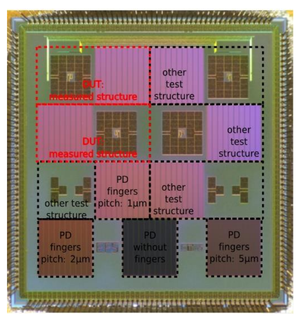
CMOS-SPAD 3D Imager



- 0.18µm CMOS technology
- < 290ps total jitter
- 11b resolution
- SPAD power < 10mW
- Frame rate:
  - 1kfps complete image
  - 100kfps interframes



CMOS ambient-light energy harvester



- 0.18µm CMOS technology
- 1.575 mm^2 die size
- 1 mm^2 solar cell
- Efficiency:
  - 25% low inputs
  - 40% high inputs