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Current Mode Techniques for Sub-pico-Ampere Circuit Design

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Abstract. In this paper we explore the low current limit that standard CMOS technologies offer for current mode based VLSI designs. We show and validate a reliable circuit design technique for current mode signal processing down to *fempto-amperes*. We will take advantage of *specific-current* extractors and logarithmic current splitters to obtain on-chip *sub-pA* currents. Then we will use a special on-chip saw-tooth oscillator to monitor and measure currents down to a few *fempto-amps*. This way, *sub-pA* currents are characterized without driving them off-chip, nor requiring expensive instrumentation with complicated low leakage setups. A special current mirror is also introduced for reliably replicating such low currents. As an example, a simple log-domain first-order low-pass filter is implemented that uses a 100 fF capacitor and a 3.5 fA bias current to achieve a cut-off frequency of 0.5 Hz and using an area of $12 \times 24.35\ \mu m^2$ in a standard 0.35 μm CMOS process. A technique for characterizing noise at these currents is described and verified. Also, temperature dependence of leakage currents is measured as well.

Key Words: leakage current, micropower, weak inversion, analog VLSI circuits, very low-time constants

1. Introduction

Reliable sub-*pA* current signal processing is a new emerging research area with several potential applications in bio-sensors, chemical sensors, image sensors for low light, applications requiring extremely long time constants, proper handling and compensation of leakage current effects (as in modern digital CMOS technologies), and many other applications yet to be discovered. CMOS is usually considered a technology for handling "low currents" like μ*-amps*. Designers experienced in weak inversion have been using *nano-amps* and smaller currents [1, 2], but rarely below 1 pA. Some publications on image sensors suggest that the lower limit for currents might be well below 1 pA [3, 4]. For example, in [4], the authors measured frequencies down to 8 mHz on an oscillator composed of a 0.1 pF capacitor and a discharging current source with voltage excursions of around one threshold voltage. This suggests that the discharge current is around 1 fA. In this paper we demonstrate that it is possible to reliably handle currents down to a few *fempto-amps* in standard CMOS, assuming one can tolerate the higher noise and mismatch which is characteristic for weak inversion [1].

The smallest MOS transistor current is limited by its leakage current. For example, using the manufacturer data in a typical present day sub-micron CMOS process, the room temperature reverse diode leakage current of the drain or source diffusions of a minimum size transistor is typically around 10 aA (10^{-17}A). However, in practical circuits this current is usually not the one that limits the lowest extent of the current range of a MOS transistor. Because of ion implantation for lowering the threshold voltage of modern CMOS technologies, the effective leakage current (i.e. for $V_{GS} = 0$) of minimum size MOS transistors may be as large as 10 pA (for the AMS 0.35 μm CMOS technology). For example, Fig. 1(b) shows the simulated I_{DS} vs. V_{GS} curves (with $V_{DS} = V_{DD}/2$, $V_{DD} = 3.3$ V) of minimum size NMOS and PMOS transistors (as seen in Fig. 1(a)), for a 0.35 μm CMOS process, using the corner analysis parameters provided by the manufacturer. As can be seen, the worst case corner yields a minimum current of around 1 pA for a minimum size PMOS and more than 10 pA for a minimum size NMOS.

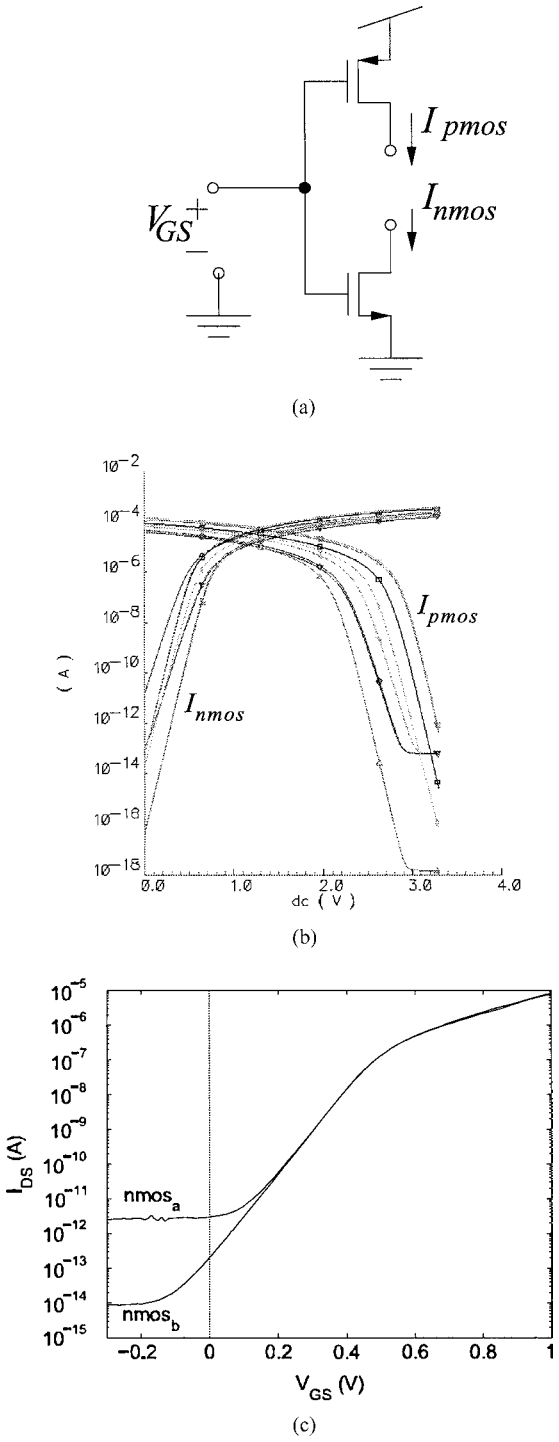

Fig. 1. Typical modern sub-micron CMOS nmos and pmos transistor I_{DS} vs. V_{GS} characteristics. (a) Schematic, (b) corner analysis simulation and (c) experimental measurements.

For $V_{GS} = 0$ V (NMOS) or $V_{GS} = V_{DD}$ (PMOS) the MOS current has not reached the diode reverse current, yielding a much larger off-current. Figure 1(c) shows two experimentally measured I_{DS} vs. I_{GS} curves. Curve nmos_a corresponds to a $W = 1\ \mu\text{m}/L = 1\ \mu\text{m}$ NMOS transistor. The minimum current of several *pico-amps* is reached for $V_{GS} \approx 100$ mV. This is the leakage current introduced by the ESD protection devices in the pads. Curve nmos_b corresponds to the parallel of 120 nmos_a transistors and dividing the measured current by 120. This way, the ESD device current is divided by 120. As can be seen, there is transistor current well below $V_{GS} = 0$ V. Therefore, biasing the gate voltages beyond the power supply rails would allow us to exploit the complete available weak inversion range down to the diffusion diodes reverse leakage currents. The key to make use of the complete available current range is by either biasing the gate voltages beyond the power supply rails (as done in Fig. 1(c)), or by slightly shifting the source voltages. For example, if for the transistors in Fig. 1 their source voltages are connected to around 400 mV with respect to the power supply rails (as shown in Fig. 2(a)), we recover the complete current range that the device physics allows us, as seen in the corner analysis simulation of Fig. 2(b). The corners with the highest leakage current (69 fA) are those obtained for high temperature (85°C). However, provided operation can be restricted to room temperatures, up to about 30°C, the lower limit for a minimum size transistor appears to be about 10 aA,[1] depending on the corner.

Source voltage shifting implies reducing the available voltage range. However, this is not a severe problem for *sub-pA* current mode circuits. Note that for such currents the gate-to-source voltage is extremely small (two or three hundreds of mV). Shifting the source voltage also implies the need of providing the on chip voltage sources V_{psh} and V_{nsh}. However, the good news are that the shifted voltage values are not critical (as long as a minimum value is guaranteed), and that the current driving capability of these on chip sources is quite low.

2. Inversion Level Based Current References

In modern CMOS processes because of threshold voltage adjustment by ion implantation there are significant variations in the position of the weak inversion I_{DS} vs. V_{GS} exponential curve (see Figs. 1(b) and 2(b)).

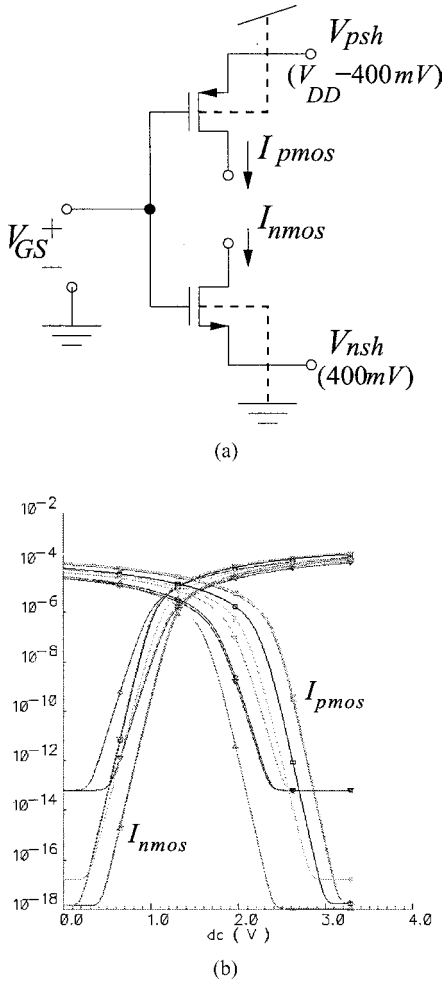

Fig. 2. Illustration of the source voltage shifting technique. (a) Circuit schematic and (b) corner analysis simulated I_{DS} vs. V_{GS} characteristics.

Consequently, biasing transistors deep inside the weak inversion region results in important variations in the required V_{GS} voltages. Furthermore, when working below *pico-amps*, a slight shift in V_{GS} voltage can turn the transistor off or produce decades of variation in the operating current. The position of the weak inversion I_{DS} vs. V_{GS} exponential curve changes significantly not only from chip to chip (or wafer to wafer) but also with temperature. Fortunately, it suffers little variations for transistors within the same die (assuming constant temperature distribution). A good solution for process and temperature independent biasing of transistors is to rely on the *Specific Current* concept and the use of on-chip *Specific Current Extractors* [1, 6].

There are MOS models in the literature [5, 6] that provide continuous analytical functions for the transistor current from weak to strong inversion, exploiting the inversion level concept. The transistor drain current is expressed as the difference between a forward I_F and reversed I_R components

$$\begin{aligned} I_D &= I_F - I_R = I_S(i_f - i_r) \\ I_S &= \frac{W}{L}\mu C'_{ox} n \frac{\phi_t^2}{2} \end{aligned} \tag{1}$$

where I_S is called "specific current", $\phi_t = KT/q$ is thermal voltage, and $i_f = I_F/I_S, i_r = I_R/I_S$ are the dimensionless inversion levels of the forward and reverse currents. Terminal voltages are related to the inversion levels by

$$\begin{aligned} V_P - V_S &= \phi_t h(i_f) \\ V_P - V_D &= \phi_t h(i_r) \end{aligned} \tag{2}$$

where $V_P \approx (V_G - V_{T0})/n$ is the pinch-off voltage and $h(\cdot)$ is a nonlinear function. For the EKV model [1] it is a mathematical interpolation

$$h(i) = 2\ln\left(\exp\left(\frac{1}{2}\sqrt{i}\right) - 1\right) \tag{3}$$

while for the ACM [6] model it was derived from physical principles

$$h(i) = \sqrt{1+i} + \ln(\sqrt{1+i} - 1) - 2 \tag{4}$$

The specific current I_S changes with process parameters and temperature. However, the ratio $g_m/(I_D\phi_t)$ depends only on the forward inversion level i_f, if the transistor is biased in saturation [5, 6]. Consequently, if one designs a circuit so that transistors operate at predetermined inversion levels then $g_m/(I_D\phi_t)$ will remain independent of process variations and temperature. To achieve this, an on chip specific current I_S extractor circuit is required. Once I_S is available, transistors can be biased with scaled versions of it, thus assuring the desired inversion levels. For weak inversion operation I_S needs not to be known with very high precision. Since there are several decades of available current range, I_S can usually be extracted with up to a factor of 2 error without significant impact. In our case, we used the circuit in Fig. 3 [7]. This circuit requires the I_3 branch to operate in strong inversion, the I_1 branch in weak inversion, and the I_2

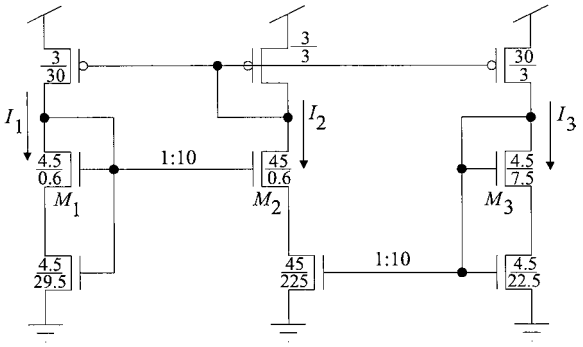

Fig. 3. Specific current extractor circuit.

branch in moderate inversion. For the sizes in Fig. 3 it auto-biases M_3 at $i_{f3} = 16$. Since M_3 is in saturation, its reverse current can be neglected resulting

$$I_3 \approx 16 I_{S3} = 16 \frac{W_3}{L_3} I_{S\square} \tag{5}$$

where $I_{S\square} = \mu C'_{ox} n \phi_t^2 / 2$ is transistor size independent. In our case we used a 0.35 μm CMOS process and designed I_3 to have a typical value of 1 μA, $I_2 =$ 100 nA, and $I_1 = 10$ nA. Corner analysis simulations reveal that the maximum to minimum current ratio for these values is less than but close to 2.

The approximate currents in the circuit of Fig. 3 are $I_1 = 1$ μA, $I_2 = 100$ nA, and $I_3 = 10$ nA. If we want to generate currents well below *pico-amps* we can use the current splitting technique [8, 9]. The circuit in Fig. 4(a) illustrates this technique. Transistors have a size ratio of either $W/L = N-1$, $W/L = N/(N-1)$, or $W/L = 1$. This way the current produced at the different output branches is progressively divided by a factor of N. In standard applications this circuit is usually used with $N = 2$, thus providing a set of binarily weighted currents, which can be controlled digitally by means of switches to produce any combination of them. In our case, we are interested in obtaining very low currents. Consequently, in order to scale down I_{REF} quickly we choose $N = 10$ and select only one of the output branches at a time. The rest of the branches are connected to a voltage source providing a path for the currents, as shown in Fig. 4(b). The 3-bit digital word w selects one output branch to connect to node I_{out}. Since w is a natural number between 0 and 7, the output current would be $I_{\text{out}} = I_{\text{REF}}/10^w$. According to Fig. 4(a), a splitter for $N = 10$ requires transistor M_f to be a unit transistor, M_a to be 9 unit transistors and M_b

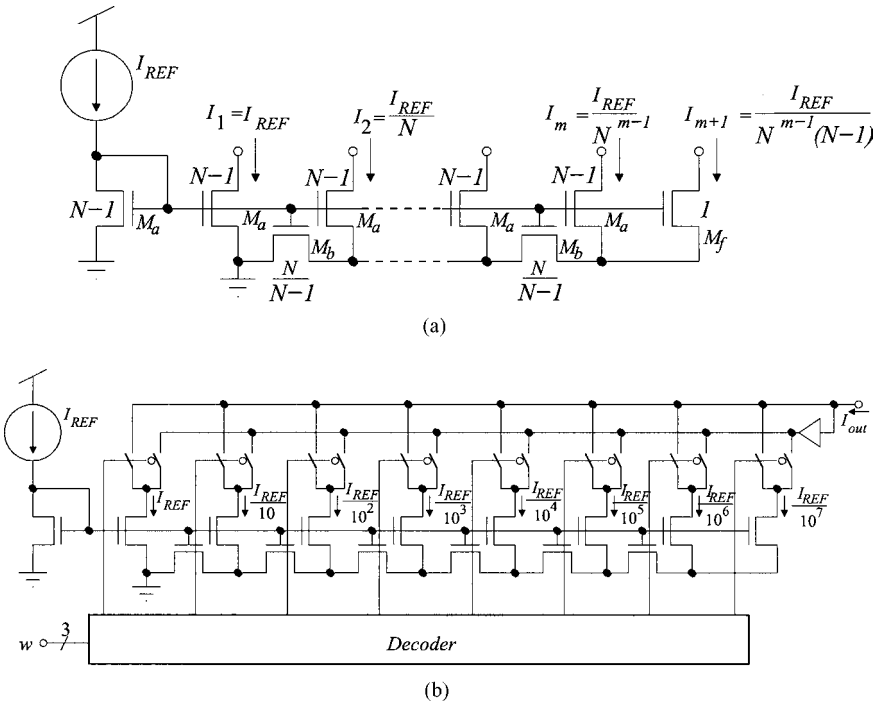

Fig. 4. (a) Circuit schematic for generic current splitting with ratio N. (b) Implemented current splitter.

to be $9 \times 10 = 90$ unit transistors. To avoid extensive leakage currents because of such a high number of unit transistors, M_b was approximated to $W_b/L_b = 1$ (one unit transistor). Therefore, consecutive output currents will not have an exact ratio of 10, although close to 10, and still we are able to scale down I_{REF} quickly to a few *fempto-amps*.

3. On-Chip Measurement of *Fempto-Ampere* Currents

Measuring *fempto-amp* currents off chip is a cumbersome and tedious task which requires expensive instrumentation and very careful wiring and handling to avoid undesired parasitic leakage. To avoid all this, we designed a simple on-chip saw-tooth oscillator driven by a current that sets its frequency of operation. The oscillator should keep operating for currents as small as the diffusion diodes reverse currents. Using such an oscillator would allow us to have a reasonable good estimate of the currents we are injecting into it. The circuit is shown in Fig. 5. Input current I_{in} discharges capacitor C_{osc}, while transistors M_1 and M_2 are OFF and M_3 is ON. Note that M_1 and M_2 have their source voltages shifted so that when their gates are connected to V_{DD} and ground, respectively, they don't drive any current (only their reversed biased drain diffusion diode currents). As the capacitor voltage reaches V_{REF} the voltage comparator output will go from low to high. The positive feedback through transistor M_2 speeds up significantly this transition [4]. After a small delay produced by the three inverters and capacitors and C_1 and C_2, transistor M_3 is turned OFF while M_1 goes ON recharging C_{osc} capacitor quickly to its starting value V_{TOP}. This will make the comparator output trip back to low, which after the inverter chain delay turns M_1 again OFF and M_3 ON. At this point input current I_{in} starts to discharge again C_{osc}. The capacitor voltage v_C at C_{osc} is monitored through a high speed analog buffer. This signal can be observed from the outside of the chip. The discharge slope at v_C is directly proportional to the discharge current I_{in}

$$slope = \frac{\Delta v_C}{\Delta t} = -\frac{I_{\text{in}}}{C_{\text{osc}}} \tag{6}$$

After measuring this slope with a known reference current (provided externally), we can infer the value of any in-chip current by comparing both slopes.

By combining the oscillator of Fig. 5 with the current splitter in Fig. 4(b) we can produce and measure

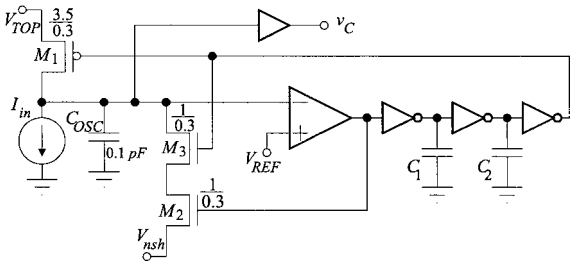

Fig. 5. Saw tooth oscillator for on chip measurement of *sub-pico-amp* currents.

extremely small currents. The reference current flowing into the current splitter was set externally to 1 nA. Extra switches are added so that the splitter output current can be driven off-chip and measured precisely (calibrated). For the maximum current ($w = 7$), the splitter output was 1.05 nA. This value is used to derive C_{osc} in Eq. (6). Consequently, once C_{osc} is known (i.e., the oscillator is calibrated), any I_{in} in Eq. (6) can be inferred by measuring the corresponding discharging slope.

Figure 6 shows the inferred currents I_{in} vs. the measured slopes for the eight possible values of the splitter control word w. The smallest inferred current was 3.51 fA, obtained when setting $w = 0$ and $I_{\text{REF}} = 0$. This current value includes the sum of all leakage currents available at capacitor C_{osc} produced by the circuitry of the oscillator and the current splitter. Figure 7 shows the oscillator inferred input currents when setting the digital control word w constant and equal to 3 while sweeping I_{REF} from 2 μA to 30 pA. Figure 8(a) shows one snapshot of waveform v_C for an oscillator input current $I_{\text{REF}} = 100$ nA and the digital control word of the current splitter set to $w = 3$. The measured slope of the oscillator in this case is 4.7 V/s. According to Fig. 6 this slope corresponds to an oscillator input current of approximately 7 pA which also corresponds to the measurement shown in Fig. 7 for $I_{\text{REF}} = 100$ nA.

Figure 8(b) shows a similar waveform but when the discharge current is 8.7 fA. As can be seen, the straight discharge line has changed to a slight exponential behavior. This suggests that, for the smallest currents, an effective resistor in parallel with the capacitor might be present. Under these circumstances the capacitor would "see" the Thevenin equivalent in Fig. 9. Assuming the capacitor is periodically discharged from $v_c = V_{\text{top}}$ to $v_c = V_{\text{bottom}}$, then

$$v_c(t) = v_{\text{eq}} + (V_{\text{top}} - v_{\text{eq}})e^{-t/(RC)} \tag{7}$$

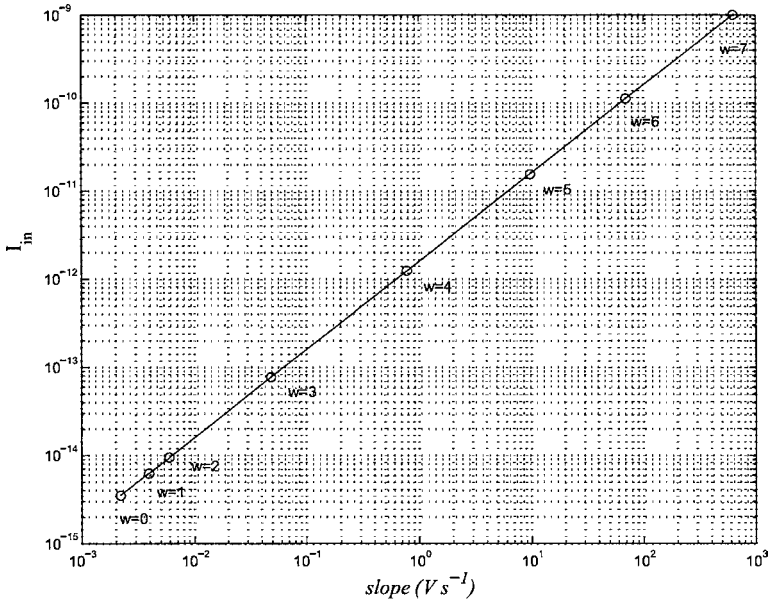

Fig. 6. Saw tooth oscillator inferred input currents versus measured slopes. $I_{\mathrm{REF}} = 1$ nA and digital control word w was set from 7 to 0.

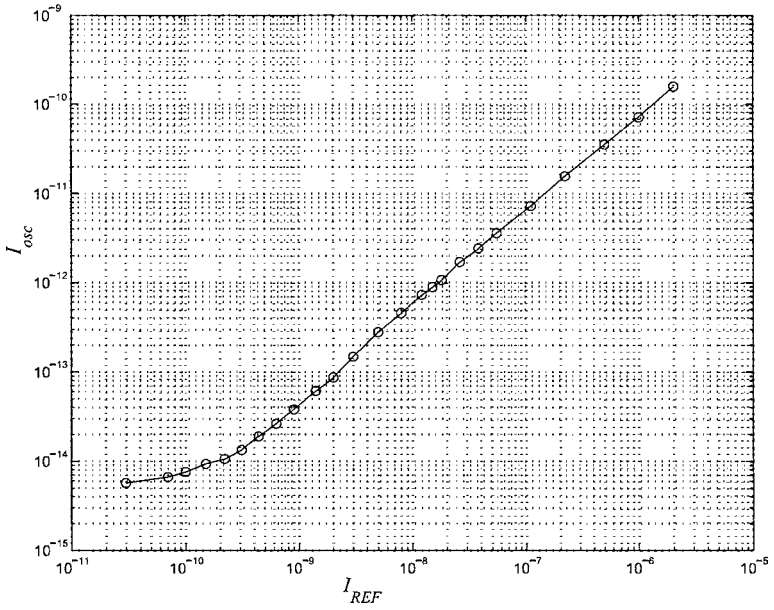

Fig. 7. Sawtooth oscillator inferred current versus I_{REF} while setting w constant equal to 3.

Adjusting the oscillator for small voltage excursions at v_c ($V_{\mathrm{top}} - V_{\mathrm{bottom}} = 0.1$ V), the effective discharge current "seen" by capacitor C would be

$$I_d \approx \frac{\bar{v}_c - v_{\mathrm{eq}}}{R} \tag{8}$$

where $\bar{v}_c$ is the average voltage at v_c during the discharge process. This equivalent discharge current can be inferred experimentally by comparing slopes and using Eq. (6), as indicated in the previous Section. By repeating this for different $\bar{v}_c$ values, the measured data point circles in Fig. 10 are obtained, which represent

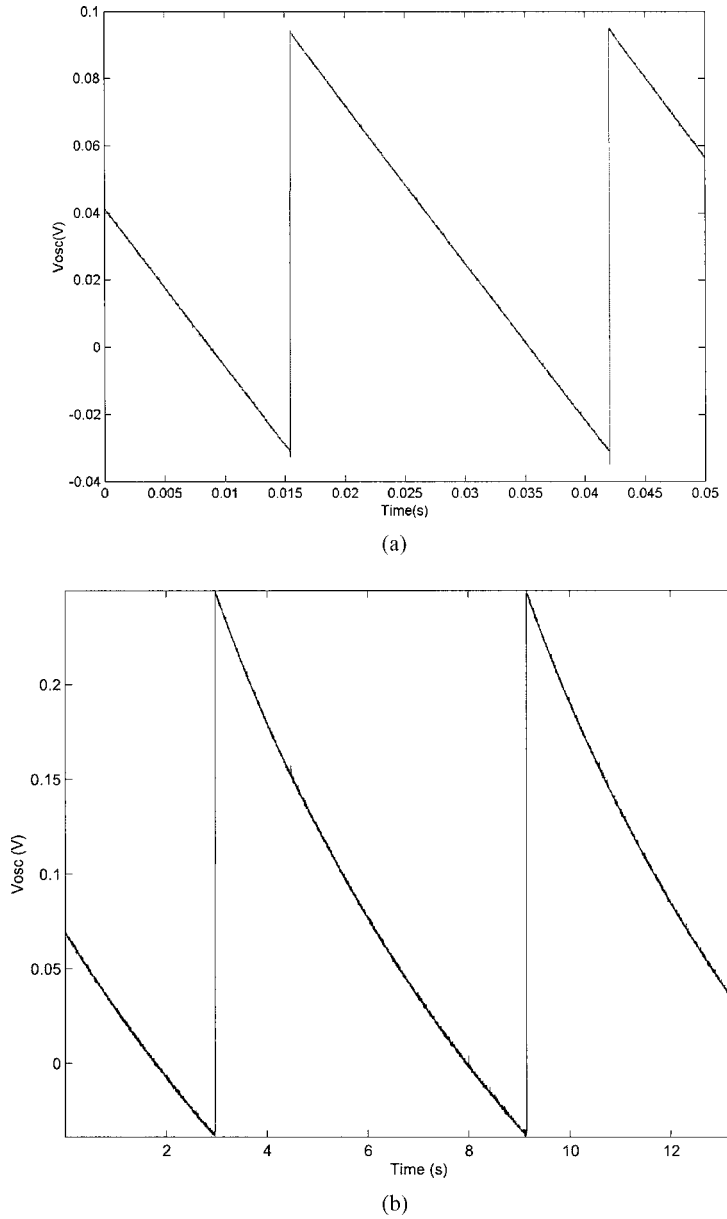

Fig. 8. Snapshots of oscillator for (a) $I_{\text{osc}} \approx 7$ pA and for (b) $I_{\text{osc}} \approx 8.7$ fA. The vertical scale shows $v_c - V_{\text{REF}}$.

I_d as a function of $\bar{v}_c$. The straight line in Fig. 10 is the result of linear regression on the data and reveals

$$\begin{aligned} R &= 34.6\ \text{G}\Omega \\ v_{\text{eq}} &= 1.75\ \text{V} \end{aligned} \tag{9}$$

This is the Thevenin equivalent of all leakages present at node v_c when the splitter is set for the minimum output current ($w = 0$) with $I_{\text{REF}} = 1$ nA, at room temperature.

4. Leakage Currents Temperature Effects

The saw-tooth oscillator will keep working as long as the net currents "seen" by capacitor C_{osc} are negative, i.e. they discharge the capacitor. Node v_c is connected

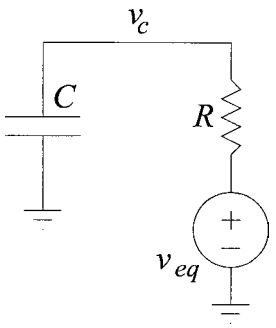

Fig. 9. Thevenin equivalent in parallel with capacitor.

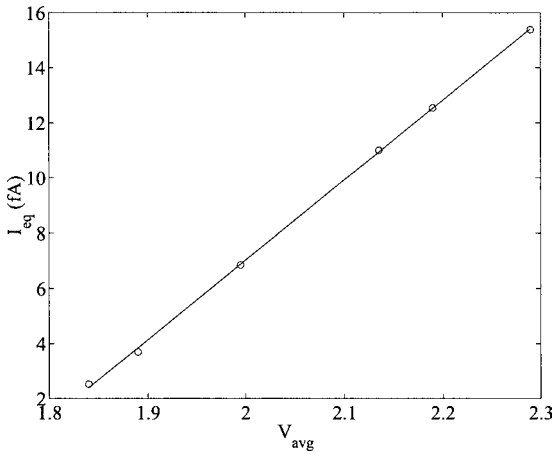

Fig. 10. Relationship between average oscillator capacitor voltage and estimated discharge current, for minimum splitter control word ($w = 0$).

to two NMOS transistor diffusions (M_3 and M_2) and a PMOS transistor diffusion (M_1). Consequently, there will be positive and negative leakage currents, and the net sum will either charge or discharge the capacitor. When all leakage currents balance out, the capacitor voltage will remain constant at voltage v_{eq}. This voltage can be measured experimentally by simply setting voltage V_{REF} in Fig. 4 sufficiently low (for example, $V_{REF} = 0$V). Figure 11 shows the dependence of this voltage with respect to temperature.

Obviously, in order to have a net capacitor discharge leakage current, the saw-tooth oscillator must be operated with a capacitor voltage v_c above v_{eq}. This is easily achieved by controlling properly the maximum and minimum voltages of v_c through V_{TOP} and V_{REF}, respectively. Under these circumstances, the saw-tooth oscillator will operate properly, and we will be able to measure the discharging slopes, and consequently the net discharging leakage current. Figure 12 shows, as a function of temperature, the net discharge currents obtained experimentally for different voltage ranges (set through V_{REF} and V_{TOP}). As discussed previously, leakage currents behave more as a leakage resistance (at least, for voltages close to v_{eq}). This fact makes the measured leakage currents in Fig. 12 to depend on the voltage range.

5. *Sub-pA* Current Mirrors

A fundamental building block for any current mode signal processing circuit is the current mirror. Figure 13(a) shows the schematic of a conventional simple NMOS current mirror. Simulating its input output characteristics by sweeping I_{in} from 10^{-17} A to 1 μA while performing corner analysis reveals the results shown in Fig. 13(b) (drain voltage of output transistor M_2 was connected to $V_{DD}/2$). The worst corner minimum operating current for this mirror is 15.6 pA, well above the worst case reverse biased diffusion diode currents (about 70 fA in Fig. 2(b)). This is because transistors cannot be turned completely OFF. Shifting the source voltages for this mirror does not solve the problem because the gate voltage cannot go below the source voltage for this topology. Using the topology in Fig. 14(a) allows the gate voltage to adapt below the shifted source voltages. Transistors $M_3 - M_5$ implement a voltage shifter that makes the gate voltage of M_1 to be one threshold voltage below its drain. Performing corner analysis simulations on this topology provides the results shown in Fig. 14(b). The high temperature corners saturate at the diffusion diodes leakage currents (69 fA), while the others remain fully operative down to 10 aA (10^{-17} A).

In order to test experimentally this current mirror topology, a PMOS and an NMOS version was used in combination with the current splitter and the saw tooth oscillator, as shown in Fig. 15. By setting signal '*select1*' high (and all others low) the current splitter output is connected directly to the saw tooth oscillator. Setting '*select2*' high (and all others low) makes this current go through the two *sub-pA* NMOS and PMOS current mirrors. By setting signal '*cal1*' high (and all others low), while setting the splitter to its maximum value, we can measure externally the maximum current provided by the splitter. This allows us to calibrate the slopes of the oscillator when it is connected directly to the splitter. By setting '*cal2*' high (and all others low),

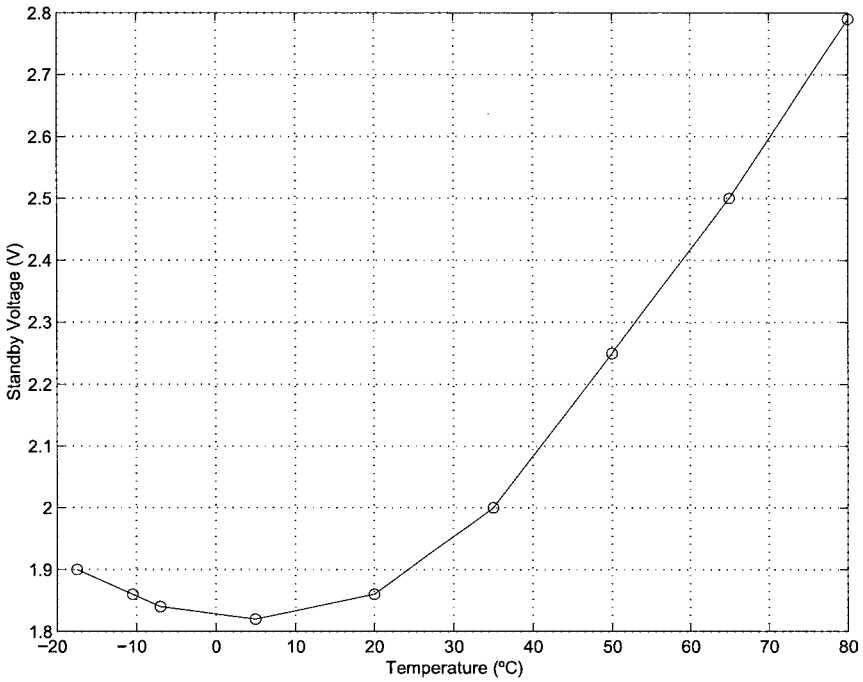

Fig. 11. Dependence of stand-by voltage v_{eq} with temperature.

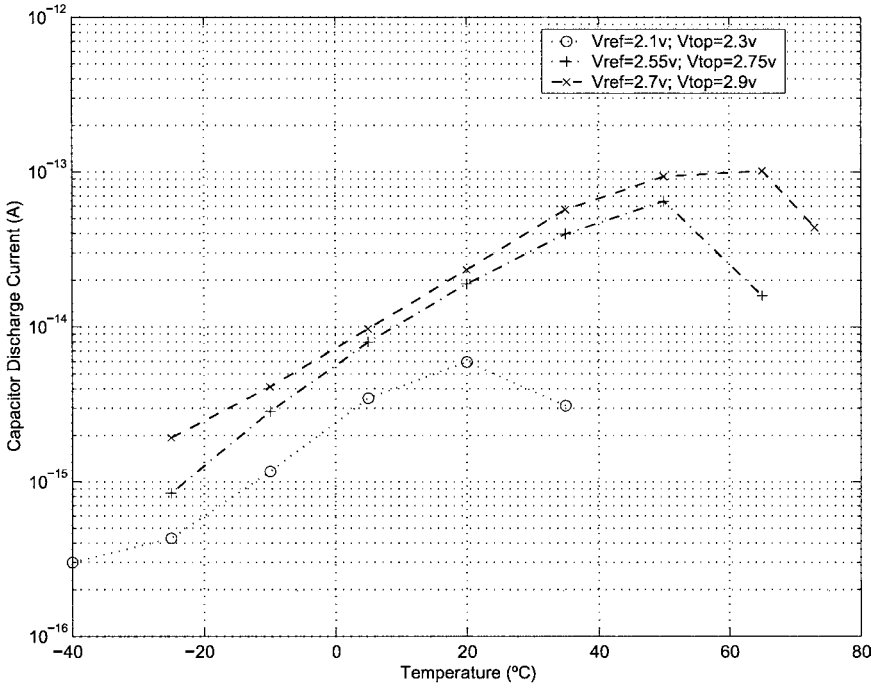

Fig. 12. Measured leakage current as a function of temperature for different voltage ranges.

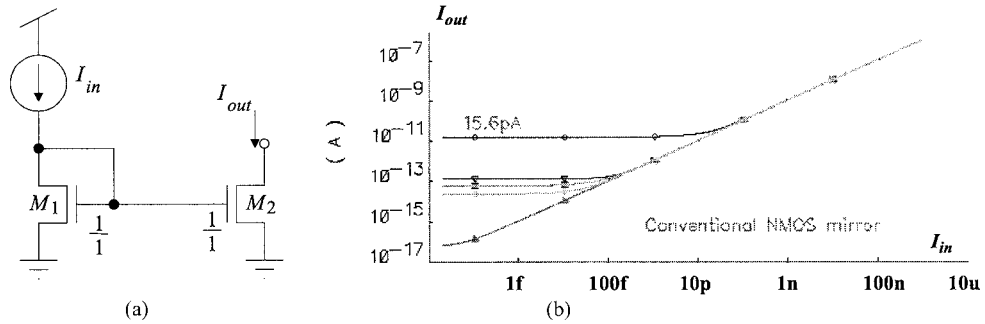

Fig. 13. Conventional simple current mirror. (a) Schematics and (b) input output current characteristics corner analysis.

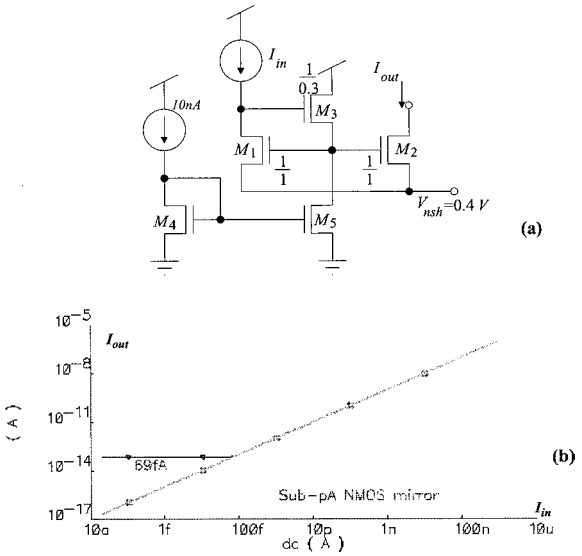

Fig. 14. New current mirror topology suitable for *sub-pA* current operation. (a) Schematics and (b) input output characteristics corner analysis.

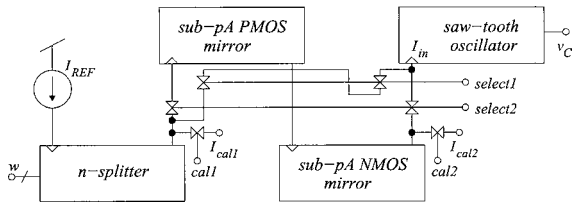

Fig. 15. Testing of *sub-pA* current mirrors using current splitters and low current saw tooth oscillator.

with the splitter at its maximum value, we calibrate the slopes for the case the two current mirrors are in the path. Note that C_{osc} in Eq. (6) is different if the mirrors are or are not in the path.

Figure 16 shows the experimental results of this new *sub-pA* current mirror topology. Figure 16(a) shows the inferred input currents in the saw tooth oscillator versus the measured slope for the two above mentioned situations: when the current splitter is directly connected to the input of the oscillator (curve marked with circles in Fig. 16(a)); and when the current goes through the combination of the NMOS and PMOS *sub-pA* current mirrors (curve marked with stars in Fig. 16(a)). From the results shown in Fig. 16(a) the curve in Fig. 16(b) can be inferred, which shows the current at the oscillator when the current splitter is connected directly to the oscillator (named as *Ics* in Fig. 16(b)) versus the input current in the oscillator when the current from the current splitter goes through the combination of the NMOS and PMOS *sub-pA* current mirrors (named as *Icm* in Fig. 16(b)). This way, curve in Fig. 16(b) represents the input current (*Ics*)-output current (*Icm*) relation of the combination of the NMOS and PMOS *sub-pA* current mirrors.

Another transistor topology appropriate for *sub-pA* current processing, since it implicitly uses source voltage shifting, is shown in Fig. 17 [10]. This topology adds the feature of clamping the mirror input voltage and improving speed response. The input voltage is clamped because of the virtual ground effect of the differential amplifier. To estimate the speed response, assume the differential amplifier acts as an instantaneous device that does not introduce any delay. If this is the case, the large signal transient response of the circuit in Fig. 17 will be

$$I_{\text{in}} = I_{M1} + \frac{C_p}{g_{oa} A_v} \dot{I}_{M1} + C_p \frac{n U_T \dot{I}_{M1}}{A_v I_{M1}} \qquad (10)$$

where A_v is the differential amplifier voltage gain, g_{oa} its output conductance, C_p the mirror input node

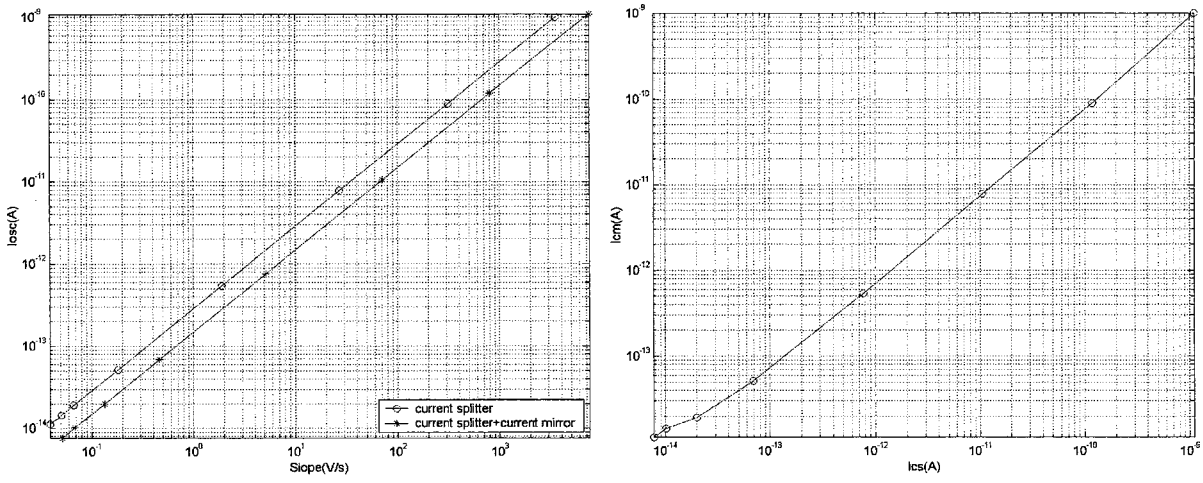

Fig. 16. Experimental results of the *sub-pA* new current mirror topology. (a) Input current inferred in the saw tooth oscillator vs. measured slopes when the current splitter is connected to the oscillator input and when the current goes through the NMOS and PMOS *sub-pA* current mirrors. (b) Inferred input-output current behavior of the compound NMOS and PMOS *sub-pA* current mirrors.

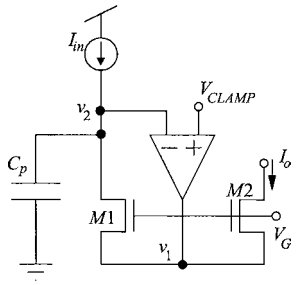

Fig. 17. A source-driven active-input current mirror with implicit source voltage shifting.

capacitance and I_{M1} the current through input transistor $M1$. If I_{in} changes in a step fashion from rI_c to I_c, the solution for Eq. (10) can be written as

$$\frac{I_{M1}(t)}{[I_c - I_{M1}(t)]^{1+\varepsilon}} = \frac{rI_c}{[I_c - rI_c]^{1+\varepsilon}} e^{t/\tau_1} \tag{11}$$

where

$$\tau_1 = \frac{C_p n U_T}{A_v I_c}, \quad \varepsilon = \frac{I_c}{g_{oa} n U_T} \tag{12}$$

If we define t_{d1} as the delay time it takes for $I_{M1}(t)$ to reach RI_c, then

$$t_{d1} = \tau_1 \ln\left[\frac{R}{r}\left(\frac{1-r}{1-R}\right)^{1+\varepsilon}\right] \tag{13}$$

Note that if A_v is sufficiently large τ_1 can be made very small, even for low values of I_c. For example, if $C_p = 0.1$ pF, $A_v = 10^4$ and $I_c = 1$ fA the resulting time constant would be 356 μs, which is a very short time interval for a circuit operating at only 1 fA current and handling a 0.1 pF capacitance.

6. Log-Domain Low-Pass Filter with Sub-Hz Cut-off Frequency

A very interesting application of *sub-pA* current mode signal processing is the capability of implementing extremely long time constant circuits without relying on large capacitances. To illustrate this, a conventional first-order log-domain CMOS filter was fabricated and tested. The schematic of the selected first order section is shown in Fig. 18 [11]. M_5 and M_6 are cascode transistors for keeping the drain voltages of M_1 and M_4 equal. The low-pass filtering function is realized by transistors $M_1 - M_4$ and capacitor C_{LPF}. Assuming all transistors in their weak inversion saturation region, the equations describing the circuit operation are

$$\begin{aligned} I_{\text{in}} I_{b1} &= I_3 I_o \\ I_3 &= I_{b2} + C_{\text{LPF}} \dot{v}_C \\ \dot{v}_C &= n\phi_t \frac{\dot{I}_o}{I_o} \end{aligned} \tag{14}$$

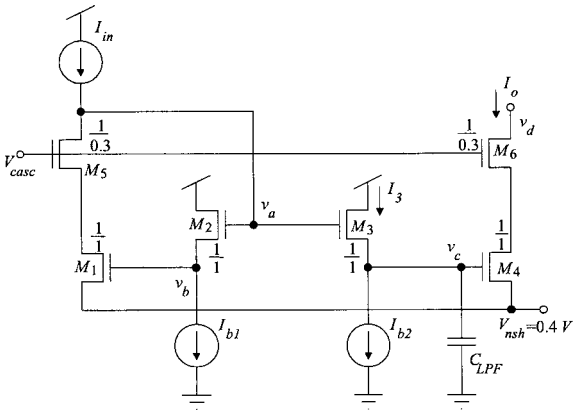

Fig. 18. Schematic of first order log-domain low-pass filter section for *sub-pA* operation.

Assuming $I_{b1} = I_{b2} = I_b$ Eq. (14) result in the following time domain differential equation

$$I_{\text{in}} = I_o + \tau_{\text{LPF}} \dot{I}_o$$
$$\tau_{\text{LPF}} = n\phi_t \frac{C_{\text{LPF}}}{I_b} \tag{15}$$

which describes a first order low-pass filter with 3 dB cut-off frequency $\omega_{\text{LPF}} = 1/\tau_{\text{LPF}}$. For a 1 Hz cut-off frequency with $C_{\text{LPF}} = 0.1$ pF, $n = 1.37$, and $\phi_t = 26$ mV, the bias current should be $I_b = 2\pi n\phi_t C_{\text{LPF}}$ $f_{\text{LPF}} = 22.4$ fA.

The log-domain low-pass filter of Fig. 18 with $C_{\text{LPF}} = 0.1$ pF was fabricated in a 0.35 μm CMOS process together with an NMOS current splitter, a saw-tooth oscillator and a set of *sub-pA* current mirrors, as shown in Fig. 19. The area of the log-domain filter is 12 × 24.35 μm. It's layout is depicted in Fig. 20.

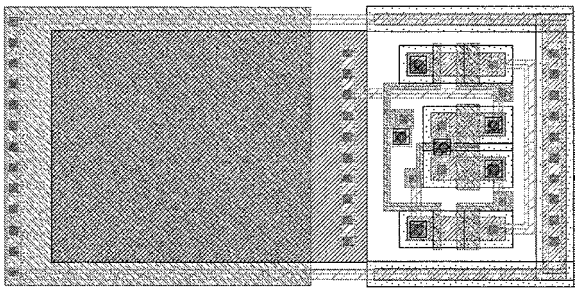

Fig. 20. Layout of the log-domain first-order low-pass filter cell in Fig. 18, with an area of 12 × 24.35 μm^2.

Current I_{REF} for the current splitter was supplied off-chip, as well as I_{be1}, I_{be2} and the two 1 MΩ resistors. I_{be1}, I_{be2}, and V_{REF} were adjusted to make the DC values $v_a = v_d$ and the low-pass transfer function was measured from v_{in} to v_o. The set-up in Fig. 19 allows us to control the value of $I_{b1} = I_{b2} = I_b$ of the low pass filter, while inferring that value by means of the saw-tooth oscillator. Figure 21 shows the measured low-pass filter frequency response for several values of I_b. Here I_{REF} was set to 1 nA and the digital control word w changed from 1 to 5. The values of the 3 dB cut-off frequency were respectively 0.5 Hz, 0.7 Hz, 1.0 Hz, 3.5 Hz, 25 Hz and 50 Hz, while I_b was inferred to be 3.51 fA, 6.25 fA, 9.53 fA, 77.8 fA, and 1.24 pA (using the saw-tooth oscillator method of Section 5). When keeping $w = 3$ constant and changing I_{REF} from 55 nA down to 70 pA the set of values $f_{3\text{dB}}$ vs. I_b of Fig. 22 were measured. Both Figs. 21 and 22 were not measured using a spectrum/network analyzer, because the frequencies were too low. Instead, input and output sinusoids were directly observed on an oscilloscope and the output waveform amplitude was manually measured as a function of input frequency.

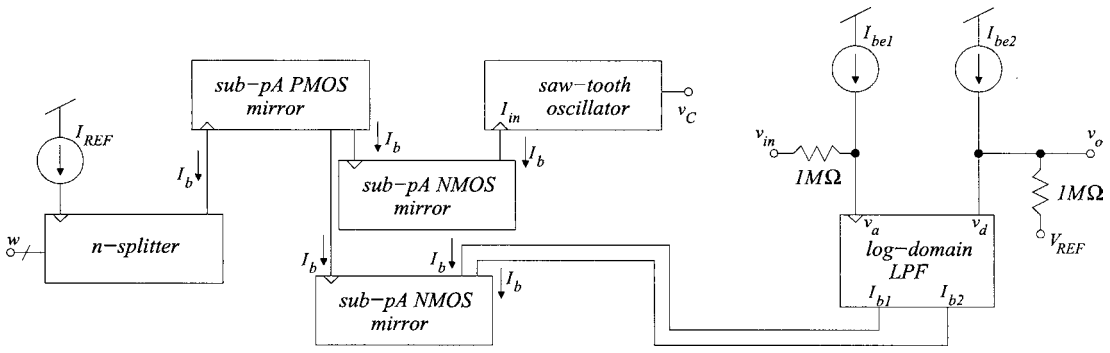

Fig. 19. Fabricated circuitry for test of *sub-pA* log-domain low-pass filter.

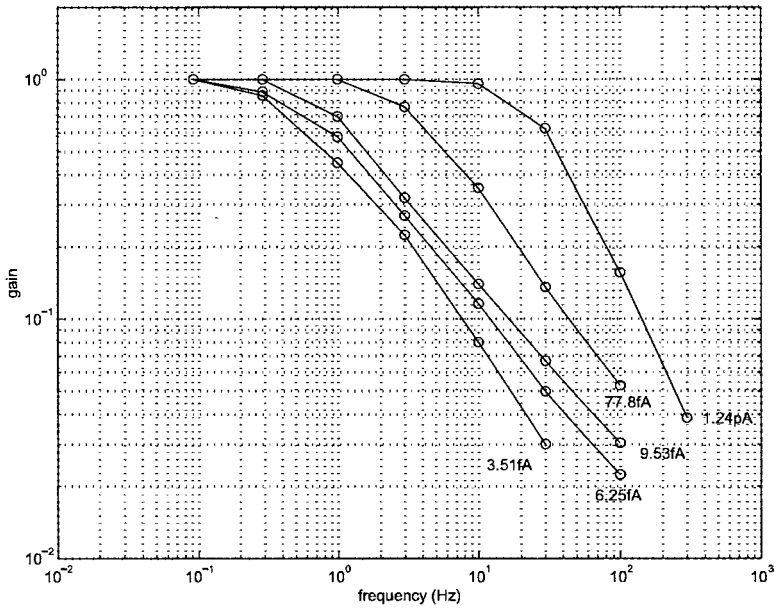

Fig. 21. Measured frequency response of the log-domain low-pass filter for different I_b values.

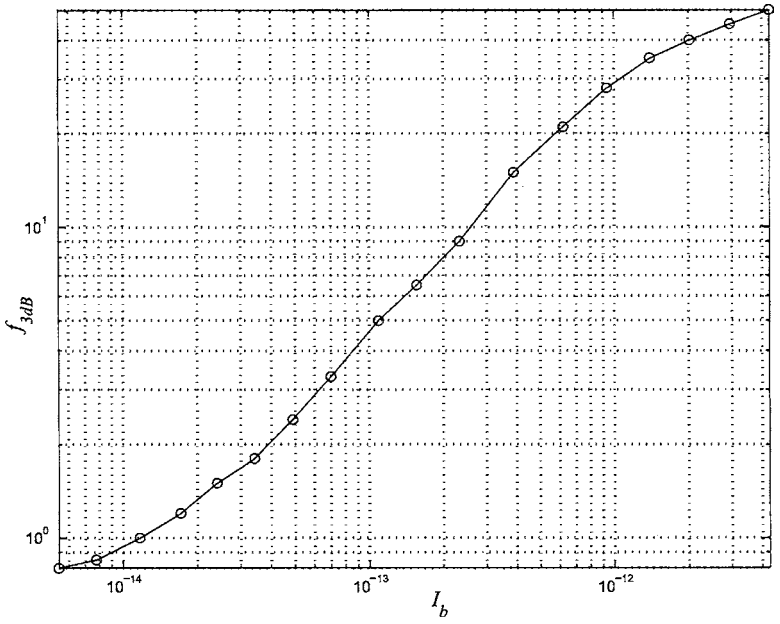

Fig. 22. Measured 3 dB cut-off frequency of low-pass filter when setting control word $w = 3$ and sweeping I_{REF} from 55 nA down to 70 pA.

7. Noise Estimation

It is possible to estimate the noise produced by the *sub-pA* MOS transistors by simply observing the saw-tooth oscillator waveforms. Measuring its frequency jitter is not a good way because it is produced not only by the input current noise but also by the comparator input equivalent noise. However, if we look at the saw-tooth oscillator wave only during the time intervals capacitor C_{osc} is being discharged, the voltage noise observed at

the capacitor is produced by the input current noise and the analog buffer noise (see Fig. 5). Designing this buffer with sufficiently low noise, the noise observed at its output will be produced by the very low currents discharging capacitor C_{osc}. Naturally, the voltage noise observed at the output will be an integrated version of the input current noise. Consequently, if the input current noise is white thermal noise, we should observe a $1/f^2$ (-20 dB/dec) output voltage noise.

To measure the noise we proceeded as follows. The oscillator waveforms were recorded using a 16-bit ADC for several values of the input current. The discharging slopes were isolated and fitted to straight lines. These lines were subtracted from the discharging slopes resulting in zero mean noise signals. These signals were analyzed using Welch's method for spectral estimation [12]. The results are shown in Fig. 23 for capacitor discharge currents equal to 7 fA, 40 fA, 600 fA, and 7 pA. Naturally, the noise spectral density could only be measured to frequencies as low as the saw-tooth frequency itself. Even more, for frequencies close to the oscillation frequency, spectral content estimation can be mistaken by distortion in the discharging slope. As can be seen in Fig. 23 all four noise measurements show the expected -20 dB per decade slope. Consequently, only white noise is being produced by the input currents for the observed frequency ranges. The thermal (white) noise power spectral density expected to be produced by weak inversion MOS transistors is [13]

$$\sigma_I^2 = 2qI \tag{16}$$

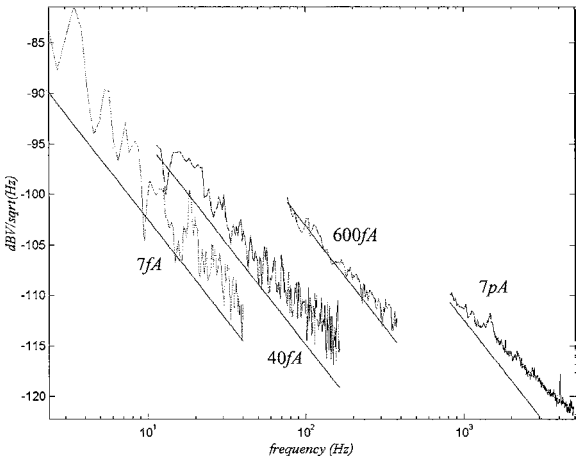

Fig. 23. Measured spectral noise density at discharging oscillator capacitor.

where q is the electron charge. Since this current noise is integrated on capacitor C_{osc} during the discharging ramps, the voltage noise present at its terminal will be

$$\sigma_V = \frac{\sigma_I}{2\pi f C_{\text{osc}}} \tag{17}$$

This theoretical noise is also shown in Fig. 23, for each discharging current, with straight lines. As can be seen, the measured noise resembles reasonably close the theoretically predicted noise.

Flicker noise ($1/f$) in subthreshold can usually be neglected with respect to thermal noise. It would, in principle, become noticeable for very low frequencies, but the $1/f$ dependence will not hold for arbitrarily low frequencies [14].

Using Eqs. (15) and (16) one can predict the signal to noise ratio (SNR) for the Low-Pass filter of the previous Section. Thus,

$$\text{SNR} = \frac{I}{\sigma_I \sqrt{\Delta f}} = \sqrt{\frac{\pi I}{q\omega_{\text{LPF}}}} = \sqrt{\frac{n\phi_t C_{\text{LPF}}}{q}} \tag{18}$$

which shows that for this filter the signal to noise ratio is current independent and depends only the size of capacitor C_{LPF}. For the fabricated prototype, it was $C_{\text{LPF}} = 0.1$ pF and $n = 1.37$, which yields SNR ≈ 40 dB, independent of current level (as long as the transistors are biased in weak inversion and one can neglect flicker noise). Note that the fabricated capacitor is fairly small, which means that SNR can be easily improved by increasing C_{LPF}.

8. Conclusions

We have shown that it is possible to design and exploit reliably *sub-pico-ampere* current mode circuits. The key is to use "source-voltage shifting." Currents in the range of pA and well below can be reliably generated on-chip by means of inversion level based *specific-current* extractors and logarithmic current splitters. To monitor *sub-pA* currents, a simple current driven saw-tooth oscillator can be included on-chip. An appropriate *sub-pA* current mirror topology has been introduced as well for proper current replication at such low values. As an application, a very simple low-pass filter has been designed, fabricated and tested. It is based on log-domain circuit techniques. It uses 6 small size transistors, a 100 fF capacitor, and provides a 3 dB cut-off frequency of 0.5 Hz when biased with 3.51 fA. Finally, it is shown how noise measurements can be easily

performed on transistors operating down to *femptoamps*, and how such measurements resemble close enough the corresponding theoretical predictions. Besides noise, mismatch considerations are also important for weak inversion operation. However, mismatch tends to stay current independent within weak inversion and it is expected that for *sub-pico-ampere* operation mismatch can be predicted with the same weak inversion models for higher currents [1, 9, 15].

Acknowledgments

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Note

1. In the simulations the current resolution was set to be 10^{-18} A.

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