A Programmable Neural Oscillator Cell

BERNABÉ LINARES-BARRANCO, EDGAR SÁNCHEZ-SINENCIO, SENIOR MEMBER, IEEE, ANGEL RODRÍGUEZ-VÁZQUEZ, MEMBER, IEEE, AND JOSÉ L. HUERTAS, MEMBER, IEEE

Abstract—**A programmable analog neural oscillator cell architecture is presented. The proposed neuron circuit is of hysteretic neural nature with its implementation based on operational transconductance amplifiers (OTA's). The hysteresis loop as well as the frequency of oscillation are voltage (or current) dependent. The architecture, which involves two OTA's, a current mirror, a capacitor, a diode, and a resistor is very suitable for monolithic integrated circuits. Experimental results confirm the expected flexibility of the synthetic neuron.**

I. Introduction

THE MOST efficient computational system is the human brain. Biological systems ordinarily perform reasoning and logical manipulations beyond the capabilities of our most modern sophisticated computer systems. Many researchers motivated by that efficiency try to mimic the human nervous system to solve a variety of complex engineering problems, among them: control systems, knowledge processing and signal/image (sensor) processing. A neural system consists of many highly interconnected neurons. Since in general neural networks involve a very large number of parallel arrays of basic cells (neurons), they are very appropriate for VLSI technology. Besides, there are some interesting applications where only a limited number of neurons are used, e.g., low-order optimization problems [1], [2], crude respirator control systems simulation [1], [3].

A biological neuron has both excitatory and inhibitory connections. Each neuron has inputs which are the outputs of other neurons as well as external (stimuli) signals, and if the sum of the inputs is greater than a certain threshold level, a firing sequence of pulses is generated, otherwise below this level the neuron will not fire. The number of pulses fired out depends on the intensity and duration of the input pulse, as well as on the inherent characteristics of the neuron.

Manuscript received June 24, 1988; revised December 20, 1988. This paper was recommended by Guest Editors R. W. Newcomb and N. El-Leithy.

B. Linares-Barranco was with the University of Seville, 41012 Seville, Spain. He is now with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843.

E. Sanchez-Sinencio is with the Department of Electrical Engineering, Texas A & M University, College Station, TX 77843-3128.

A. B. Rodriguez-Vasquez and J. L. Huertas are with the Department of Electronics and Electromagnetics, Faculty of Physics, University of Seville, 41012 Seville, Spain.

IEEE Log Number 8826710.

Synthetic neurons behave in a crude similar way to the actual neurons. In this paper, a programmable neuron circuit architecture is presented. The implementation is based on the operational transconductance amplifier (OTA), this voltage (or current) programmable device is very suitable for synthetic neurons. The proposed neuron circuit is of the hysteretic neural-type pulse oscillator [4] with the inhibitory and excitatory properties as function of the input sum exceeding (or not) a firing threshold level.

II. Mathematical Description of a Hysteretic Neuron

A basic first-order state-variable type equation [1], [4] simulating (in a primitive way) a neuron is given by

$$C\frac{dx}{dt} = -G_x x - G_H H(x) - G_u u \tag{1a}$$

$$y = x \tag{1b}$$

where u = input, y = output, x = internal state variable; C, G_x, G_H, and G_u are non-negative constants, and $H(x)$ describes the hysteresis nature of the neuron model

$$H(x) = \begin{cases} H_+, & \text{if } x > x_+ \\ -H_-, & \text{if } x < -x_- \\ \{H_+, -H_-\}, & \text{if } -x_- < x < x_+ \\ [-H_-, H_+], & \text{if } x = -x_- \text{ or } x = x_+ \end{cases} \tag{2}$$

Observe that there are other neuron models with similar mathematical characterization. For instance, the term $-G_H H(x)$ in other characterizations [2], [5] is related to $-\sum_{j=1}^{p} D_{ji} f_j(x)$ where D_{ji} is a weighting function, and $f_j(\cdot)$ are nonlinear functions imposing constraints and can be considered as threshold-activation functions.

In what follows, we rewrite (1) in a form most useful for our circuit implementation, i.e.,

$$C\frac{dx}{dt} = -G_x(u)x + I_o(x) \tag{3a}$$

$$y = x \tag{3b}$$

where $I_o(x)$ is $-G_H H(x)$, and the input variable u con-

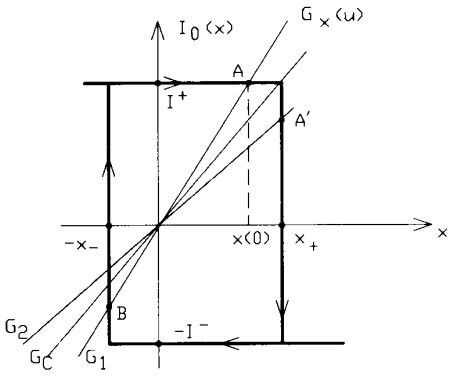


Fig. 1. Equilibrium point characteristics.

trols the value of $G_x(u)$, and the $-G_u u$ term has been deleted. The equilibrium points are obtained when $dx/dt = 0$, this yields

$$I_o(x) = G_x(u)x. \tag{4}$$

The intersections of the hysteresis function $I_o(x)$ with resistive (load-line) $G_x(u)x$ provide the equilibrium points, as shown in Fig. 1. It can be observed from Fig. 1 that point A is a stable point, and point B is an unstable point. The asymmetry of the hysteresis loop is needed to guarantee only one stable point. For our circuit implementation we need a mechanism to change the slope $G_x(u)$ such that the straight line moves from point A to point A' and becomes unstable when u becomes excitatory. Hence, the circuit oscillates and fires negative pulses when the input signal u exceeds a certain threshold level; this package of pulses is terminated when u falls below threshold. Thus, there is a critical value G_C which separates points like A and A', e.g.,

$$\begin{aligned} &G_x(u) > G_C \text{ stable point } A \\ &G_x(u) < G_C \text{ unstable point } A'. \end{aligned} \tag{5}$$

Fig. 2 illustrates the time response of this neuron for a current pulse $u(t)$ that makes $G_x(t)$ to jump between G_1 and G_2 so that $G_2 < G_C < G_1$. This input pulse makes the stable equilibrium point A to change to point A' which is unstable. At the initial time of change of u the output of the hysteretic element starts at I^+, and, since x cannot change instantaneously, the differential equation characterizing the neuron yields

$$C\frac{dx}{dt} = -G_2 x + I^+ \text{ with } x(0) = \frac{I^+}{G_1}. \tag{6a}$$

Hence, the time solution initially is given by

$$x(t) = I^+\left[\frac{1}{G_2} + \left(\frac{1}{G_1} - \frac{1}{G_2}\right)e^{-(G_2/C)t}\right]. \tag{6b}$$

This equation holds until $x(t)$ becomes $x_+ = I^+/G_C$, at which time the output of the hysteretic element changes to $-I^-$ (we assume the ideal case where no time is taken in going from I_+ to $-I_-$ on the hysterisis curve) and let t_0 be this time, with $x(t_0) = I^+/G_C$. Therefore solving for t_0

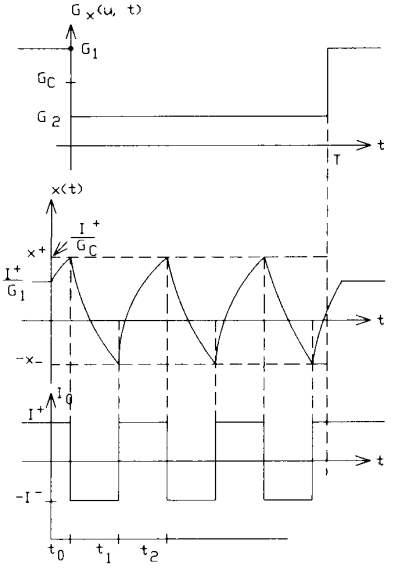


Fig. 2. Characteristic time response of neuron cell.

we obtain

$$t_0 = \frac{C}{G_2}\ln\left(\frac{1 - G_2/G_1}{1 - G_2/G_C}\right). \tag{7}$$

Now the characterizing differential equation becomes

$$C\frac{dx}{dt} = -G_2 x - I^- \text{ with } x(0) = \frac{I^+}{G_C} \tag{8}$$

which solution is given by

$$x(t) = -\frac{I^-}{G_2} + \left(\frac{I^+}{G_C} + \frac{I^-}{G_2}\right)e^{-(G_2/C)t}. \tag{9}$$

This situation is maintained until $x(t)$ becomes $-x_-$, and $I_0(x)$ then changes back to $+I^+$ to return to point A and, hence to complete the cycle that will generate a neural-type pulse output. Thus

$$x(t_1) = -x_-. \tag{10}$$

Solving for t_1 yields

$$t_1 = \frac{C}{G_2}\ln\frac{1 + \dfrac{I^+ G_2}{I^- G_C}}{1 - \dfrac{G_2}{I^-}x_-}. \tag{11}$$

Now the differential equation becomes (6a) again

$$C\frac{dx}{dt} = -G_2 x + I^+ \text{ but with } x(0) = -x_- \tag{12a}$$

and the solution is given by

$$x(t) = \frac{I^+}{G_2} - \left[x_- + \frac{I^+}{G_2}\right]e^{-(G_2/C)t}. \tag{12b}$$

The time at which $I_0(x)$ changes from I^+ to $-I^-$ occurs

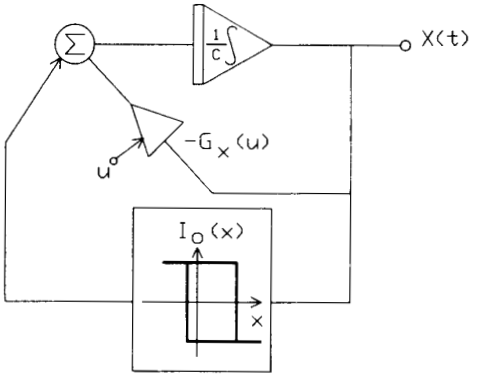


Fig. 3. Block diagram of neural-pulse simulator.

when in (12b)

$$x(t_2) = \frac{I^+}{G_C} \tag{13}$$

thus t_2 results

$$t_2 = \frac{C}{G_2} \ln \frac{1 + G_2 \frac{x_-}{I^+}}{1 - G_2/G_C}. \tag{14}$$

If T is the duration of the input pulse u and n_p is the number of pulses generated by the neuron, the next inequalities hold:

$$t_0 + (n_p - 1)(t_1 + t_2) < T < t_0 + n_p(t_1 + t_2). \tag{15}$$

Hence, if one were to hold G_x constant at $G_2 < G_C$ then the number of pulses that would occur while G_2 remains constant is

$$n_p = \text{Int}\left(\frac{T - t_0}{t_1 + t_2}\right) + 1 \tag{16}$$

where $\text{Int}(\cdot)$ produces the integer part of the function $((T - t_0)/(t_1 + t_2))$.

III. A Proposed Neural Pulse Simulator

A block diagram of the proposed neural-type circuit which implements (3a) and (3b) is shown in Fig. 3. In our circuit, the outputs of the hysteretic element $I_0(x)$ and of the externally controllable linear amplifier $G_x(u)$ are currents, while their inputs are voltages. Accordingly, the integrator is built with a simple capacitor and the current summer element simply implements *KCL* and, hence needs no additional circuitry.

In order to implement the transconductance hysteretic element to yield $I_0(x)$, we used a differential input transconductance comparator with multiple outputs all taking values

$$I_h(v_i) = \begin{cases} I_{\text{bias}} = I^+, & 0 < v_i \\ -I_{\text{bias}} = -I^-, & v_i < 0 \end{cases}$$

as shown in Fig. 4. An antimetric transconductance-hysteretic element can be implemented as shown in Fig. 5 where $R = 1/G_C$, and G_C is as defined before. Furthermore,

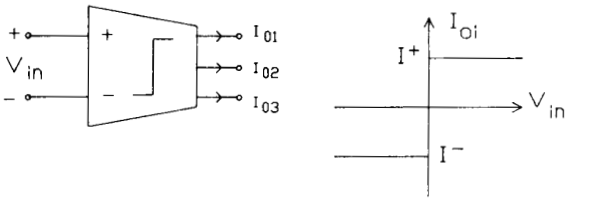


Fig. 4. A transconductance comparator with multiple outputs.

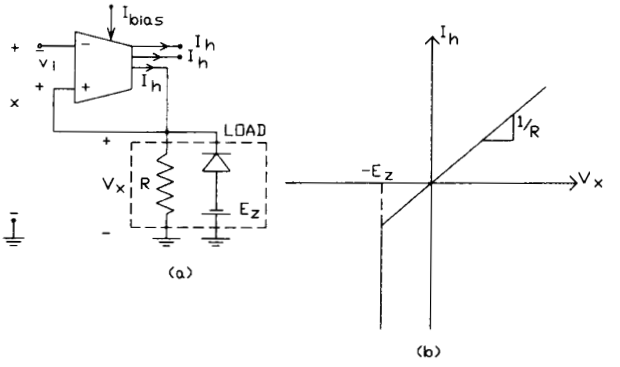


Fig. 5. Antimetric transconductance-hysteretic element. (a) Circuit implementation. (b) Characteristics of load.

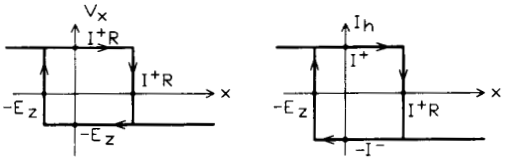


Fig. 6. Hysteresis characteristics of circuit of Fig. 5.

observe that since $v_i = V_x - x$

1) if $x < V_x$ then $v_i > 0$ and $I_h = I^+$ which back biases the diode, giving $V_x = I^+R$ and $x < I^+R$;
2) if $x > V_x$ then $v_i < 0$ and $I_h = -I^-$ and if further we choose $E_z < I^-R$ then $V_x = -E_z$ and $x > -E_x$;

where $I^+ = I^- = I_{\text{bias}}$ [8]. I_{bias} is the controlling current of the OTA. These observations are summarized in Fig. 6. The other element needed to build up the block diagram of Fig. 3 is an externally current controlled linear transconductance amplifier. A conventional OTA is employed [8], [9]. The transconductance gain G_x is controlled by the bias current u. This is shown in Fig. 7.

Now we can put together the basic elements to form the *programmable neural oscillator cell* as shown in Fig. 8. The equation describing the behavior of the circuit of Fig. 8 is given by (3) for which x is chosen as the capacitor voltage, $I_o(x)$ has $I^+ = I^- = I_{\text{bias}}$, and $G_x = hu$ with u the bias current in the bottom OTA in Fig. 8, and h [9] is a proportional constant which depends upon temperature, device geometry, and the process.

Neurons are interconnected through synapses. A synapse can be considered as a weighted relation between the output of a neuron and the input received by another one.

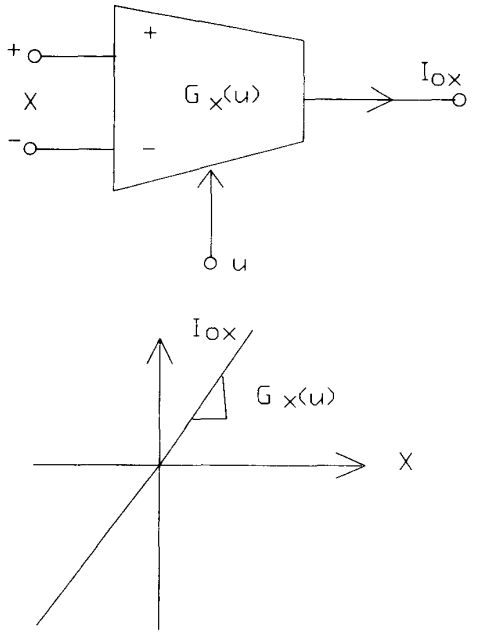


Fig. 7. A linear transconductance amplifier.

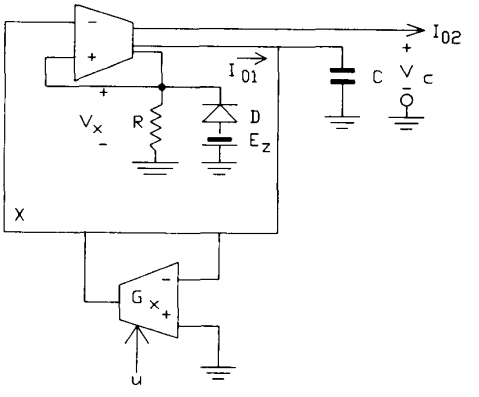


Fig. 8. A hysteretic neural cell implementation.

This relation can be inhibitory or excitatory. In the proposed neuron circuit, the negative current pulses can be arbitrarily considered to be excitatory signals, while other positive current pulses could be considered the inhibitory signals. This excitatory and inhibitory property of the neuron circuit can be implemented as an integrated circuit version by means of complementary current mirrors for taking output of one neuron to feed other neurons.

IV. Experimental Results

The circuit of Fig. 8 was built as a test protoboard. The commercial transconductance devices used were the VA703 OTA's. For the linearized OTA implementing $G_x(u)$, the linearizing diodes [8] provided within the chip were used as well as an additional resistive attenuator to increase the input voltage swing. The input linear range obtained was about ± 3 V for a ± 5-V power supply.

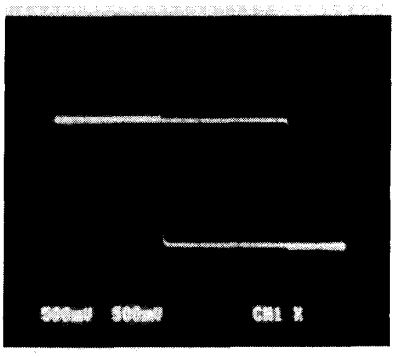


Fig. 9. Hysteresis loop measurement.

For the transconductance comparator with multiple outputs, three OTA's (VA703) were used. These three OTA's had their inputs and bias connected together so that they would work like an OTA with three equal outputs. The input impedances of both transconductance devices (the comparator and the linearized one, G_x) are not very high, so a voltage buffer had to be added. The values (arbitrarily chosen) of the passive elements were $R = 1.8$ kΩ and $C = 33$ nF.

The measured hysteresis loop of I_{01}[1] versus x is depicted in Fig. 9. The bias current of the comparator was adjusted to $I_{\text{bias}} = 0.8$ mA, and the voltage $E_z = 0.5$ V.

The upper trace of Fig. 10(a) shows the output current of the neuron ($I_{02} = I_{01} = I_h$) of Fig. 8 when the input u is a square wave (shown in the lower trace) of 4.4 mA. This square wave makes the transconductance of $G_x(u)$ to jump from $G_1 = 7.7 \times 10^{-4}$ mho (stable point) to $G_2 = 1.6 \times 10^{-4}$ mho, (unstable point) being the width of the pulse (excitation time) $T = 900$ μs. The critical point of $G_x(u)$ is given by $G_C = 1/R = 5.6 \times 10^{-4}$ mho.

If T, C, G_1, G_2, G_C, I^+, and E_z are known, we can calculate the values of t_0, t_1, t_2, (via (7), (11) and (14)) as well as the number of pulses n_p fired during the excitation time T (eq. (16)).

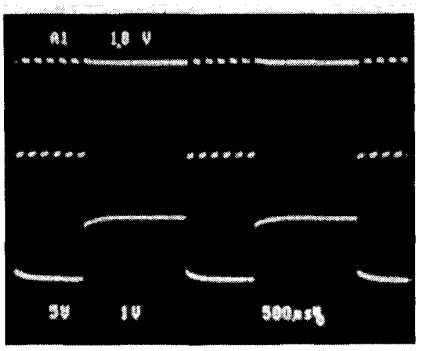
The calculated values are

$$t_0 = 22\ \mu\text{s}$$
$$t_1 = 75\ \mu\text{s}$$
$$t_2 = 89\ \mu s$$
$$n_p = 6.$$

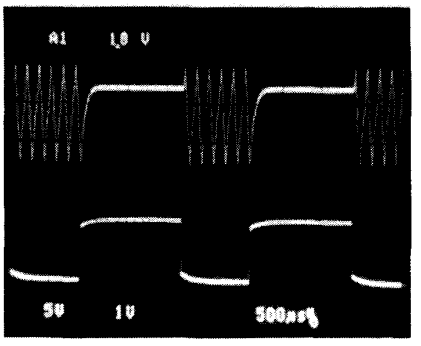
It can be seen from the upper trace of Fig. 10(b), where the voltage across capacitor C is shown for the same input signal u as in Fig. 10(a) that the experimental values of the previous calculated times are approximately:

$$t_0 = 24\ \mu\text{s}$$
$$t_1 = 80\ \mu\text{s}$$
$$t_2 = 94\ \mu\text{s}$$
$$n_p = 6.$$

[1] I_{01} was measured across a resistor of 1.0 kΩ.



(a)



(b)

Fig. 10. (a) Current time response V_x/R for a square wave input current u. Time response V_C for a square wave input u.

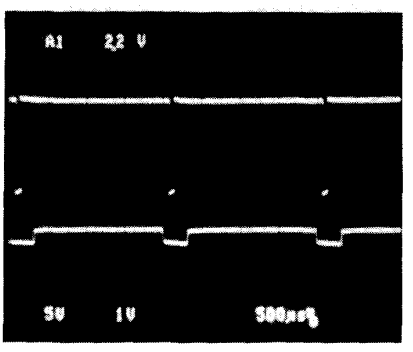


Fig. 11. Same as Fig. 10(a) with smaller amplitude and duration of u.

The difference between measured and calculated values is less than 10 percent, which can be due to component tolerances and parasitic elements.

Fig. 11 shows the output response V_x of circuit of Fig. 8 when the input signal becomes a pulse of smaller magnitude and duration, ($T \simeq 300$ μs and $n_p = 1$ since $(T - t_0)/(t_1 + t_2) < 1$.

V. Conclusions and Future Work

An analog synthetic neuron architecture with voltage (or current) programmable properties has been presented. In fact, referring to Fig. 8, the proposed architecture has two degrees of freedom (I_{bias} and u) to modify the neuron output; they are functions of the two OTA's which can be voltage (or current) dependent. This current dependence modifies $H(I^+)$ and G_x in (1). If needed, the weight of the interconnections between neurons (synapses) could be determined by means of current mirrors. The addition of current signals from other output neurons or external stimulus at each neuron circuit is accomplished through the controlling terminal of the OTA's (i.e., see signal u).

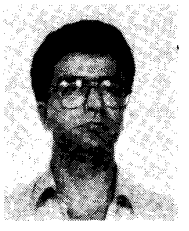
Contrary to some other analog neural circuits where it is difficult to change their parameters [6], this neuron architecture has additional flexibility to modify its parameters according to a certain predetermined algorithm. We are currently working on the MOS integrated version of the proposed neuron architecture taking into account area [7], flexibility, and power consumption.

Acknowledgment

The authors wish to thank Professor R. W. Newcomb for his valuable comments, suggestions, and encouragement in the preparation of this paper.

References

[1] F. C. Hoppensteadt, *An Introduction to the Mathematics of Neurons*. New York: Cambridge Univ. Press, 1986.
[2] D. W. Tank and J. J. Hopfield, "Simple neural optimization networks: An A/D converter, signal decision circuit, and a linear programming circuit," *IEEE Trans. Circuits Syst.*, vol. CAS-33, pp. 533–541, May 1986.
[3] C. Von Euler, "Central pattern generation during breathing," *Trends in Neurosci.*, pp. 275–277, Nov. 1980.
[4] G. Kiruthi, R. C. Ajmera, R. Newcomb, T. Yami, and H. Yazdani, "A hysteretic neural type oscillator," in *Proc. IEEE/ISCAS*, vol. 3, pp. 1173–1175, May 1983.
[5] A. F. Murray and A. V. W. Smith, "Asynchronous VLSI neural networks using pulse-stream arithmetic," *IEEE J. Solid-State Circuits*, vol. 23, pp. 688–697, June 1988.
[6] C. Koch, J. Marroquin, and A. Yuille, "Analog 'neural' networks in early vision," in *Proc. Natl. Acad. Sci. (Biophysics)*, vol. 83, pp. 4263–4267, June 1986.
[7] N. El-Leithy and R. W. Newcomb, "Hysteresis in neural-type circuits," in *Proc. IEEE/ISCAS*, vol. 2, pp. 993–996, June 1988.
[8] VTC Incorporated, "*High Performance Integrated Circuits*," *Data Book* (supplement) 1987.
[9] R. L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits Devices Mag.*, vol. 1, pp. 20–32, Mar. 1985.
[10] B. Linares-Barranco *et al.*, "A novel CMOS analog neural oscillator cell," to be presented at the ISCAS, May 1989.



Bernabé Linares-Barranco received the B.Sc. degree in electronic physics in 1986, and the M.S. degree in microelectronics in 1987, from the University of Seville, Spain. Currently, he is with the Department of Electrical Engineering, Texas A&M University, Texas, where he is working towards the Ph.D. degree.

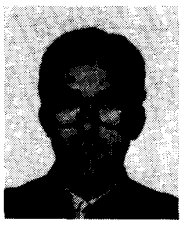
His research interest is in the area of nonlinear analog microelectronic design and neural networks.

Edgar Sánchez-Sinencio (S'72–M'74–SM'83) received the M.S.E.E. degree from Stanford University, CA, in 1970, and the Ph.D. degree from the University of Illinois, Champaign-Urbana, in 1973.

In 1974, he held an industrial Post-Doctoral position with the Central Research Laboratories, Nippon Electric Company Ltd., Kawasaki, Japan. From 1976 to 1983 he was the Head of Instituto Nacional de Astrofísica, Optica y Electrónica, Puebla, Mexico. He was a visiting professor in the Department of Electrical Engineering at Texas A&M University during the academic years of 1979–1980 and 1983–1984, where he is currrently a Professor. He was the General Chairman of the 1983 16th Midwest Symposium on Circuits and Systems. He was an Associate Editor of *IEEE Circuits and Systems Magazine* (1983–1985), *IEEE Circuits and Devices Magazine* (1985–1988) and of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1985–1987). He is the co-author of the book, *Switched-Capacitor Circuits* (Van Nostrand-Reinhold, 1984). His current research interest include operational transconductance amplifiers and applications, computer-aided design of solid-state circuits and neural network circuit implementations.

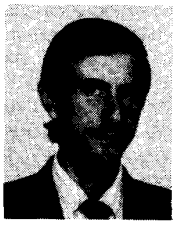
✠

Angel Rodríguez-Vázquez (M'80) received the Licenciado en Física and the Doctor en Ciencias Físicas degrees from the University of Seville, Spain, in 1977 and 1983, respectively.



Since October 1978, he has been with the Departamento de Electricidad y Electrónica at the University of Seville, where he is currently employed as an Associate Professor. His research interest lies in the fields of analog/digital integrated circuit design, neural networks and nonlinear networks analysis and synthesis.

✠



José L. Huertas (M'74) received the Licenciado en Física and the Doctor en Ciencias Físicas degrees from the University of Seville, Spain, in 1969 and 1973, respectively.

From October 1970 to September 1971, he was with the Philips International Institute, Eindhoven, The Netherlands, as a Post-Graduate Student. Since October 1971, he has been with the Departamento de Electricidad y Electrónica at the University of Seville, where he became Assistant Professor in 1973 and a Professor in Electronics in 1981. His research interest lies in the field of multivalued logic, sequential machines, analog circuit design, and nonlinear network analysis and synthesis.