The Active-Input Regulated-Cascode Current Mirror

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***Abstract*—A continuous-time current mirror circuit is presented that combines an active input and a regulated cascode output. The current mirror offers a high accuracy over an operating current range higher than previous structures. Results are demonstrated through Hspice nominal and Monte Carlo simulations.**

I. Introduction

In recent years the circuit design community has focused considerable attention on the design of signal processing circuits based on current mode principles. The attractive features of this design technique are high speed and small area with a reasonable degree of precision. Compact and fast A/D converters [1], filters [2], neural networks [3], and fuzzy processing components [4] have been reported with current mode circuits.

The basic building block in a current-mode based circuit is the current mirror. Its small size and simplicity is responsible for the high speed and compactness of the resulting current-mode circuits. A widely accepted accuracy limit for a current mirror is the 8-bits (~0.4%) barrier, although for large transistor areas and currents 9-bits (~0.2%) are achievable. However, such a precision is usually achievable only for a short range of operating current and a limited range of voltage drop at the input and/or output of the current mirror. When building current-mode signal processing systems, it is often times desirable to have current mirrors that operate with this accuracy over an extensive current range (around one decade or more). In this paper we present the *active-input regulated-cascode current mirror* and show how this mirror can maintain a high accuracy degree over a wider current range, as well as for larger voltage drops.

II. Circuit Description

The active current mirror idea (see Fig. 1(a)) [1] was introduced as necessary to maintain a constant voltage at the input of a current mirror in order to avoid current subtraction errors in previous stages. This technique allows the V_{GS} voltage of the current mirror input transistor $M1$ to be independent of its V_{DS} voltage, which will be kept constant and therefore lowering the mirror input impedance and minimizing loading effects on previous stages. The current mirror will be operative as long as transistors $M1$ and $M2$ are kept in saturation. The higher the reference voltage V_D is, the more current is allowed through the mirror with $M1$ operating in saturation. The drain-to-source voltage of the output transistor depends on the load of the mirror and will be dependent on the mirror current. If the load impedance is not sufficiently, low $M2$ will suffer large drain-to-source voltage variations, which through the channel length modulation effect will cause a systematic mismatch error between the input and output currents of the mirror. Such a circumstance can be avoided by using the cascode current mirror of Fig. 1(b). However, this mirror has a smaller output voltage swing and requires a high input voltage drop for high currents (which are needed for maximum accuracy) [5]. The regulated-cascode output stage (see Fig. 1(c)[1]) [6] would allow to maintain the V_{DS} of transistor $M2$ constant XXX and to increase significantly the output impedance of the mirror, while not sacrificing voltage range at the input of the current mirror. This current mirror will be operative as long as transistor $M2$ remains in saturation, which depends on V_D and the input current, as well as on the load impedance at the output of the mirror.

By combining the active current mirror input of Fig. 1(a) with the regulated-cascode output in Fig. 1(c), *the active-input regulated-cascode current mirror* of Fig. 1(d) results. This current mirror has a very low input impedance, a very high output impedance and is operative if transistors $M1$ and $M2$ are either in saturation or ohmic region (because their V_{DS} voltages are always equal). Therefore, the gate voltage of transistors $M1$ and $M2$ can change from rail to rail. However, this current mirror will fail to operate with high accuracy if the output voltage approaches V_D. But, on the other hand, V_D can be made smaller than for Fig. 1(a) because $M1$ and $M2$ can operate now in ohmic regime.

When cascading current mirrors, the regulated-cascode output is not needed and the configuration of Fig. 1(a) can be used. The virtual ground effect at the drain of transistor $M2$ is produced by the active input of the next current mirror. However, in this case V_D has to be set equal for all PMOS and NMOS active current mirrors. Also, care has to be taken by choosing the value of V_D in order to respect the output voltage range of the circuit at the input of the first mirror and to respect the input voltage range of the circuit at the output of the last current mirror.

III. Accuracy Considerations

The accuracy limitation of current mirrors has two main types of sources, systematic errors and random errors. Systematic errors are caused by different V_{DS} voltages at transistors $M1$ and $M2$ due to poor input/output impedance coupling between subsequent stages and high-order nonlinear effects. Random errors are fundamentally caused by differences in the electrical parameters between transistors $M1$ and $M2$, due to random process parameter variations. While random mismatch error contributions are practically independent on the circuit topology, systematic errors change considerably from one topology to another. We will consider that the total precision of a current mirror is given by

$$\Delta I_{\text{Total}} = \Delta I_{\text{sys}} + \sigma_I \tag{1}$$

where ΔI_{sys} is the systematic error contribution (evaluated through a single nominal Hspice simulation) and σ_I is the standard deviation of the output current (evaluated through 30 Hspice Monte Carlo simulations). The statistical significance of σ_I is that 68% of the samples have an output current error within the range $(\Delta I_{\text{sys}} - \sigma_I, \Delta I_{\text{sys}} + \sigma_I)$. For random mismatch errors Hspice simulations it is considered that the only sources of random mismatch are the differences in threshold voltage (V_T) and current factor ($\beta = C_{\text{ox}}\mu W/L$) and that their standard deviation is given by [5]

$$\sigma^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2 \tag{2}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2$$

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[1] Although we are showing a differential input voltage amplifier, in the original paper [6] a single input amplifier was used. In this case the voltage V_D would be set through process and circuit parameters.

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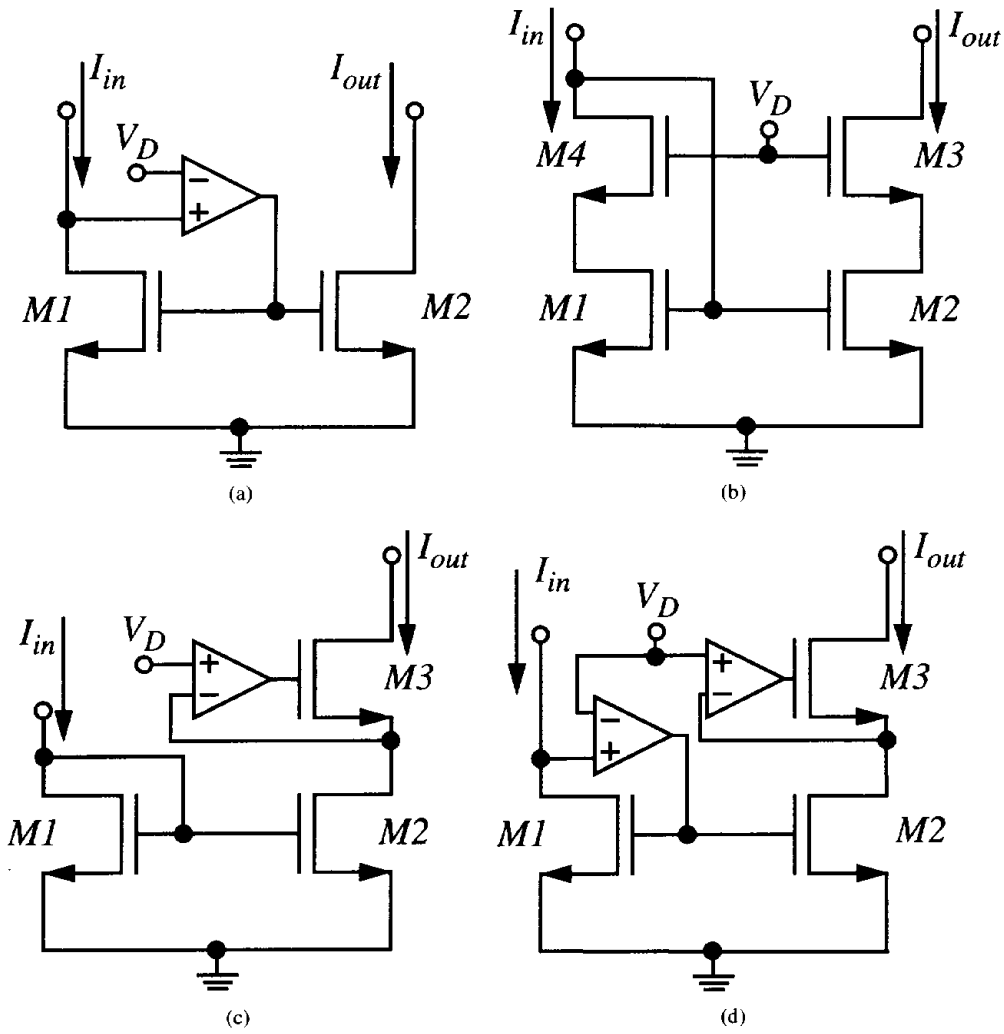

Fig. 1. Enhanced current mirror topologies. (a) active, (b) cascode, (c) regulated cascode output, and (d) active regulated cascode.

where W and L are the sizes of the transistors, D ($\sim W$) their separation and $A_{VT} = 15$ mV μm, $S_{VT} = 2$ μV/μm, $A_\beta = 2.3\%$ μm, $S_\beta = 2 \times 10^{-6}$ μm (parameters given in [5] for a 1.6 μm N-well process with 25 nm gate oxide and direct wafer writing).

In the following simulations we use $W = 100$ μm and $L = 20$ μm for transistors $M1$ and $M2$ of all current mirror topologies, with $V_D = 1.5$ V (power supply is 5 V). Fig. 2 represents the total accuracy of (1) as a function of operating current for different current mirror topologies. The first two topologies are for the *active-input regulated-cascode current mirror* with amplifier gain values $A = 1000$ and $A = 100$. For $A = 1000$ the resolution is above 8-bits for current values between 40 μA and 750 μA, while for $A = 100$ it is only between 40 μA and 330 μA. In both cases the decrease in precision above ~300 μA is because transistors $M1$ and $M2$ enter their ohmic region of operation. A simple current mirror has a resolution below 8-bits for the complete current range. This is mainly due to poor impedance coupling, which can be avoided with regulated cascode outputs, achieving 8-bits resolution between 45 μA and 150 μA. The cascode mirror suffers from large voltage drops at its input, thus offering the 8-bits resolution only between 40 μA and 70 μA. The active-input mirror (Fig. 1(a)) has low resolution because its output voltage was set to 2.5 V, hence rendering an important systematic error contribution. Also shown in Fig. 2 is the random mismatch error contribution (σ_I in (1)), which is approximately the same for all the topologies. Note that all topologies suffer from loss of precision at high currents. This is produced because the increasing voltage drops at the different nodes approximate the limit of available voltage range.

IV. Stability and Speed Considerations

The use of the active input requires stability compensation [1]. Compensation of an active-input current mirror for an operating current of several decades and achieving speed figures better than for standard current mirror topologies is not a simple task. For our application, where we needed to achieve 8-bits accuracy for a one-decade operating current and with speeds faster than 100 ns (for most part of the range), we required the use of an automatic transistor sizing optimization tool [7] for the design of the voltage amplifiers. For our application we required voltage amplifiers with a gain lower than 1,000, therefore a simple topology could be used ([1] or [8]). The regulated cascode output amplifier does not require compensation.

Table I shows the transistor level simulated transient times of our design when using a regular OTA [8] as the active device. These transients correspond to the time the mirror takes to settle to 1% of the final current value, when the input is driven by an ideal current step signal changing between the levels given in the first row of the table. Table I also shows the delays for other topologies that have the same transistor sizes. Note that speed is improved with respect to mirrors that do not use active devices. The reason is that the

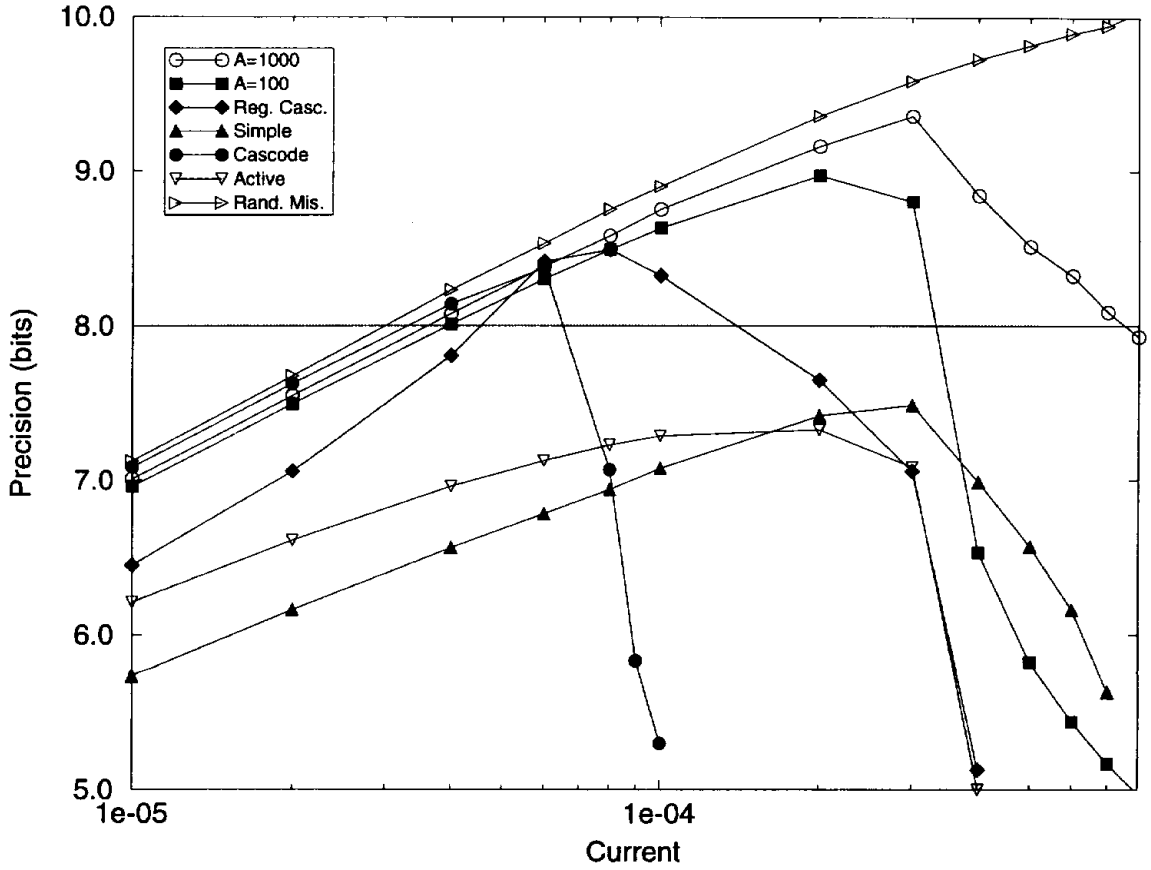

Fig. 2. Resolution (in bits) as a function of working current for different current mirror topologies.

TABLE I

	10μA to 15μA	50μA to 75μA	100μA to 150μA	250μA to 375μA	400μA to 600μA	530μA to 800μA
act. reg. casc.	65ns	70ns	45ns	45ns	70ns	460ns
simple	160ns	80ns	65ns	40ns	80ns	35ns
cascode	180ns	85ns	-	-	-	-
active input	65ns	70ns	45ns	35ns	45ns	-
reg. cas. out.	165ns	80ns	65ns	50ns	-	-

active device introduces more design variables, thus allowing a more optimum final result.

V. Conclusion

In this paper we present a very simple current mirror idea, that results from the combination of two independent previous contributions [1], [6]. This idea served our purposes in a specific current-mode processing application where we needed a set of fast current mirrors able to deliver an 8-bits precision with a one-decade of operating current range. No other current mirror topology was able to meet these specifications.

References

[1] D. G. Nairn and C.A.T. Salama, "Current-mode algorithmic analog-to-digital converters," *IEEE J. Solid-State Circ.*, vol. 25, pp. 997–1004, Aug. 1990.

[2] S. S. Lee, R. H. Zele, D. J. Allstot, and G. Liang, "CMOS continuous-time current-mode filters for high-frequency applications," *IEEE J. Solid-State Circ.*, vol. 28, pp. 323–329, Mar. 1993.

[3] A. Rodríguez-Vázquez, S. Espejo, R. Dominguez-Castro, J. L. Huertas, and E. Sanchez-Sinencio, "Current-mode techniques for the implementation of continuous- and discrete-time cellular neural networks," *IEEE Trans. Circ. and Syst.*, vol. CAS-40, pp. 132–146, March 1993.

[4] T. Kettner, C. Heite, and K. Schumacher, "Analog CMOS realization

of fuzzy logic membership functions," *IEEE J. Solid-State Circ.*, vol. 28, pp. 857–861, July 1993.

[5] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circ.*, vol. 24, pp. 1433–1440, Oct. 1989.

[6] E. Säckinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circ.*, vol. 25, pp. 289–298, Feb. 1990.

[7] F. Medeiro, R. Rodríguez-Macias, F. V. Fernández, R. Domínguez-Castro, J. L. Huertas, and A. Rodríguez-Vázquez, "Global design of analog cells using statistical optimization techniques,"*Analog Integrated Circuits and Signal Processing*, to be published Oct. 1994.

[8] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circ.*, vol. SC-17, no. 3, pp. 522–528, June 1982.