IV. Results and Comparisons

Tests have been executed to measure the distortion introduced by RCMF in real images and to compare its performance with that of MF. Comparisons have been carried out in terms of *Mean Absolute Error* (MAE) which is known to reflect image fidelity, as it appears to a human viewer, better than the usual *Mean Square Error* [6].

Noisy versions of the test image *Harbor* have been produced by randomly replacing a fraction p of its pixels with equi-probable black and white values. MAE distortion is reported in the plots of Fig. 2, for both RCMF (Fig. 2(a)) and MF (Fig. 2(b)) as a function of p, for different square window sizes. As it appears, MAE lower than for MF at any p evidence the reduced amount of distortion introduced by RCMF; higher degree of preservation is achieved for window sizes larger than for MF, as suggested in Section II. Due to the rank-conditioning, the minimum distortion is not attained for $p = 0$, but when a certain percentage of noisy (i.e., *boundary*) values falls within the filter window. Fig. 3 shows original and an extremely noisy version ($p = 0.5$), the 5×5 MF and 7×7 RCMF processed images. The two window sizes for MF and RCMF have been chosen so as to jointly optimize the noise suppression and detail preservation capabilities of both. It is noteworthy that RCMF is superior in terms of spatial accuracy not only of edges and fine details, but also in textures (sea with waves) and in uniformly smooth regions (sky), thus establishing the theoretically derived features.

V. Conclusion

A novel median filtering scheme exploiting a rank-dependent decision rule has been proposed for low-distortion impulsive noise removal. Theoretical investigations have proven the enhanced *salt and pepper* noise suppression capability with respect to median filter. Also, the increased spatial accuracy of the response is assessed both visually and by Mean Absolute Error comparisons between *noise-free* and processed image versions.

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A Modular Current-Mode High-Precision Winner-Take-All Circuit

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***Abstract*— Traditional Winner-Take-All (WTA) circuits rely on the matching of an array of N transistors, where N is the number of inputs of the WTA [1], [2]. This implies that when N increases, also increases the size of the WTA and the distance between the transistors that have to match, which yields to transistor matching degradation and loss of precision in the overall WTA circuit performance. Furthermore, when multi-chip WTA's are required, transistor matching is even worse, and the performance is drastically degraded. In this paper we present a WTA circuit technique, based on current-mode principles, that does not rely on matching of a transistor array. The operation of the circuit depends on current transport and replication by local current mirrors with a small number of outputs. Thus N can increase and the precision is not degraded, not even if the WTA is disbrituted among several chips. Even more, the different chips that constitute the WTA can be of different foundries, and the precision of the WTA is not drastically degraded. Simulation results on these facts are provided.**

I. Circuit Implementation

The present WTA circuit (or MAX operator) realizes the following equation,

$$I = \sum_{i=1}^{N} \alpha_i U(I_i - I) \tag{1}$$

where $\{I_i\}$ is a set of positive constant inputs (whose maximum we are seeking), α_i are positive parameters that satisfy $\alpha_i \geq I_i$, and $U(\bullet)$ is the step function, defined as the limit

$$U(x) = \lim_{\varepsilon \to 0} \frac{1}{1 + e^{-x/\varepsilon}} \tag{2}$$

The solution of (1) is given by the intersection of the curves $f_1(I) = \sum \alpha_i U(I_i - I)$ and $f_2(I) = I$, called A in Fig. 1. At point A we have that $I|_A = \max_i\{I_i\}$.

Fig. 2 shows a circuit with N input-cells and one N-outputs PMOS current mirror. Each input cell (composed of a current comparator, a 2-outputs NMOS mirror, and one NMOS switch) realizes the operation $I_{oi} = I_i U(I_i - I)$. The PMOS current mirror collects and distributes the sum $I = \sum_i I_{oi}$. Thus, the circuit of Fig. 2 solves (1) for the case $\alpha_i = I_i$.

As N increases (and so does the number of transistors in the PMOS mirror) the PMOS mirror can be partitioned into a cascade (or tree) of current mirros (all of them with small inter-transistor distances), and thus avoiding a fast mirror output current matching degradation. Fig. 3 shows this for the case the PMOS mirror is split between several chips.

II. Stability Considerations

In order to analyze the stability of the WTA, we will first derive the stability conditions for a one-input WTA based on small signal circuit analysis, then extend it to the N-inputs case, and finally perform a large signal global stability analysis. Fig. 4 shows the circuit, and its small signal equivalence, of a one-input WTA. The delay elements

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TABLE I
MONTE CARLO SIMULATED PRECISION FOR PROPOSED MODULAR CURRENT-MODE WTA

I_{in}	1 μA			5μA			10 μA			50 μA			100 μA		
Case	mean	sigma	error	mean	sigma	error	mean	sigma	error	mean	signma	error	mean	sigma	error
A	997.38 nA	36.81 nA	0.04%	4.9908 μA	97.1 nA	0.11%	9.9839 μA	162 nA	0.18%	49.937 μA	657 μA	0.73%	99.882 μA	1.28 μA	1.41%
B	916.36 nA	253.54 nA	0.34%	4.9913 μA	153 nA	0.16%	10.008 μA	254 nA	0.26%	50.157 μA	977 nA	1.15%	100.31 μA	1.85 μA	2.18%

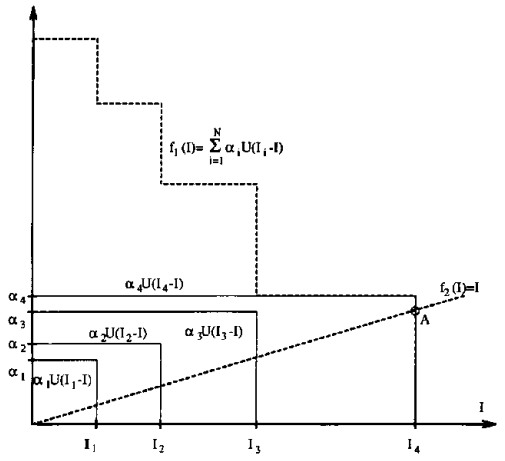

Fig. 1. Graphical representation of a particular case of (1).

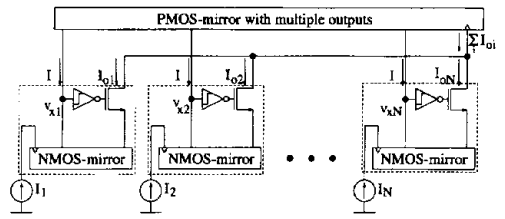

Fig. 2. Circuit diagram of complete WTA circuit.

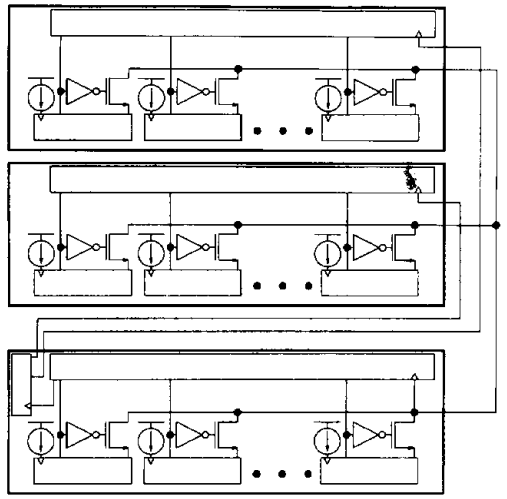

Fig. 3. Interchip connection strategy for current-mode WTA circuit.

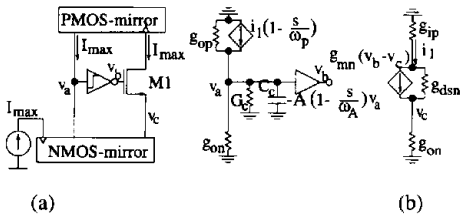

Fig. 4. One-input WTA current-mode circuit. (a) circuit diagram, (b) small-signal equivalent circuit.

that have been considered are: a) current comparator input node capacitance C_c, b) delay of current comparator ω_A, and c) delay of PMOS current mirror ω_p. Analysis of the small signal equivalent circuit of Fig. 4(b) yields the following second order characteristics equation,

$$s^2 + s\left(\frac{\omega_A\omega_p}{A}\frac{C_c}{g_{on}} - \omega_A - \omega_p\right) + \omega_A\omega_p = 0 \tag{3}$$

which yields a stable behavior if $C_c/(Ag_{on}) > \omega_A^{-1} + \omega_p^{-1}$. If the required value for C_c is excessively large, a Miller capacitor of value $C_m = C_c/A$ can be connected between the output and input of each current comparator. For an N-inputs WTA, the worst stability case occurs when all the inputs are equal $I_i = I_{max}$. In this case all NMOS switches would be ON, and each driving the fraction current I_{max}/N. Small signal stability analysis would yield the condition $C_c/(NAg_{on}) > \omega_A^{-1} + \omega_p^{-1}$. Global large signal stability analysis [3] can be performed if $C_c/(NAg_{on}) \gg \omega_A^{-1} + \omega_p^{-1}$, so that the N-inputs WTA becomes a system with a dynamics of order N. In this case, the following set of first order nonlinear differential equations describes the transient behavior of the circuit,

$$C_c\dot{v}_{xi} = G_c(v_{xi} - v_M) - I_i + \sum_{j=1}^{N} I_j U(v_M - v_{xj}) \tag{4}$$

where v_M is the trip voltage at the comparators input, and $U(\bullet)$ is given by (2) with ε small but nonzero. This circuit has the following Liapunov function,

$$E = \frac{1}{2}\sum_{ij} I_j U(v_{xi} - v_M)U(v_{xj} - v_M) + G_c\sum_i \int_0^{U(v_{xi}-v_M)} U^{-1}(\vartheta)\,d\vartheta + \sum_i \left(I_i - \sum_j I_j\right)U(v_{xi} - v_M) \tag{5}$$

which satisfies,

$$\dot{E} = -C_c\sum_{i=1}^{N} U'(v_{xi} - v_M)\dot{v}_{xi}^2 \le 0 \tag{6}$$

Since E is bounded from below, the system described by (4) is globally stable, and will reach its unique equilibrium point (see Fig. 1).

III. SIMULATION RESULTS

Simulations have been performed on the extracted netlist of an 18-inputs WTA layout designed for a 1.5 μm double-metal CMOS process. The design is intended to yield a 1.5% (6 bits) resolution at a maximum current of 100 μA. Simple current mirror topologies have been used with transistor sizes $W_n = 8.0$ μm, $L_n = 8.4$ μm (for

TABLE II
MONTE CARLO SIMULATED PRECISION FOR WTA REPORTED IN [2]

input	1.5 V			2.5 V			3.5 V			4.5 V		
Case	mean	sigma	error	mean	sigma	error	mean	sigma	error	mean	sigma	error
A	1.4975 V	9.14 mV	0.39%	2.4972 V	9.26 mV	0.40%	3.4971 V	9.32 mV	0.41%	4.4967 V	48.50 mV	1.73%
B	1.5572 V	8.35 mV	2.62%	2.7328 V	8.33 mV	9.65%	3.8185 V	8.01 mV	13.1%	-	-	-

the NMOS mirrors), $W_p = 14.4\ \mu$m, $L_p = 5.6\ \mu$m (for the PMOS mirrors). For the current comparator a simple digital inverter can be used, although we preferred a four transistor circuit [4] to improve speed. For compensation purposes, a 0.5 pF Miller capacitor around the current comparators was sufficient to stabilize our circuit. Table I shows the precision attained as a function of the input current level, measured through Monte Carlo simulations, and using the statistical parameters reported by Pelgrom *et al.* [5]. For each input current I_{in}, one WTA input was held constant at I_{in} and another was swept around this value, measuring the point at which the transition ocurred. All other inputs were maintained at $I_{\text{in}}/10$. Table I provides *mean* values, and their standard deviations (*sigma*), of the transition points for several values of I_{in}. The *error* was computed by,

$$error = \frac{|I_{\text{in}} - mean| + sigma}{range} \times 100 \tag{7}$$

being $range = 99\ \mu$A. Table I provides two rows of results: *Case A* has been obtained using the electrical Hspice model of a 1.5 μm CMOS process, and *Case B* has been obtained by splitting the WTA (see Fig. 3) between two chips of different technologies (1.5 μm CMOS and 2.0 μm CMOS of two different foundries) and preserving the same transistor sizes for both chips. In order to minimize the error in the *mean* values, high precision current mirrors have been used [6], [7]. Note that there is very little precision degradation in *Case B*. This is the main advantage of the present WTA with respect to previously reported ones. As an illustration, Table II shows the same simulated results for the WTA reported in [2] and with similar transistor sizes. Note the significant precision degradation between *Case A* and *Case B* for this WTA.[1] Table III provides simulated speed figures for the case where the proposed current-mode WTA is fully contained in a single chip, and with one input held at I_{in} while the other changes in a step fashion between $1/2I_{\text{in}}$ and $3/2I_{\text{in}}$.

[1] In Table II, for the case B and an input voltage of 4.5 V the circuit was already out of range.

TABLE III
SIMULATED TRANSIENT TIMES FOR PROPOSED WTA CIRCUIT

Iin	1 μA	5 μA	10 μA	50 μA	100 μA
delay	1.30 μs	500 ns	250 ns	120 ns	100 ns

IV. CONCLUSION

A new approach to the WTA operation has been proposed, based on current transport, replication, and comparison. This approach avoids the need to match N transistors in an array, as do conventional WTA circuits. Furthermore, the WTA can be split among several chips without significant loss of precision, even if they have been fabricated by different foundries. The only condition for nondegradation of the precision is to have locally good current mirrors. Simulation results have been provided that prove theses facts, and theoretical stability conditions for the circuit have been given.

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