Figs. 1 and 2 show that the squaring permutation produces almost the same performance as non-permutation decoding while it reduces considerably the required number of computations. The amount of the reduction is much larger in (15, 9) RS codes than (7, 3) RS codes. This shows that that the squaring permutation can be more effective as the code length increases. The reason is that, as the Galois field is larger, more squaring sequences are available.

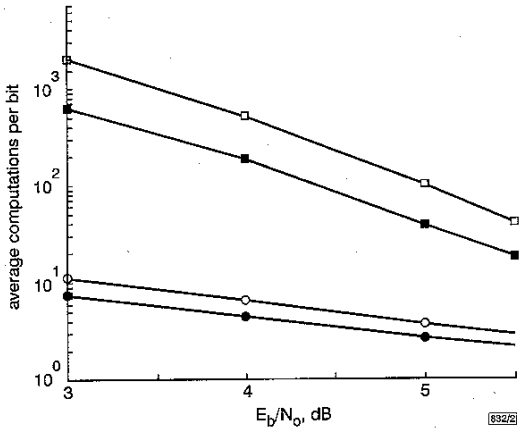


**Fig. 2** Complexity comparison using 16 level soft decision values

○—○ non-permutation for (7,3) RS codes
●—● squaring permutation for (7,3) RS codes
□—□ non-permutation for (15,9) RS codes
■—■ squaring permutation for (15,9) RS codes

In general, sequential decoding will be most effective for error patterns affecting only the parity check part of the sequence. For widely distributed errors, cyclic permutation cannot achieve this [5]. In the special case that the worst error pattern has occurred, the $m$ different permutation sequences can be very useful in finding a better starting point for cyclic permutations.

*Conclusion:* Sequential decoding can be combined with a squaring permutation on the normal basis so that the bit-level soft-decision information is preserved. The permutations give new sequences for decoding on the original trellis that cannot be generated by the previously reported cyclic permutation. Finally the combination of squaring and cyclic permutations is expected to be effective in obtaining low-complexity decoding with near maximum likelihood decoding.


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### References

1 JACOB, I., and BERLEKAMP, E.: 'A lower bound to the distribution of communication for sequential decoding', *IEEE Trans. Inform. Theory*, 1967, **IT–13**, pp. 167–174
2 SAVAGE, J.: 'The distribution of the sequential decoding computational time', *IEEE Trans. Inform. Theory*, 1966, **IT–12**, pp. 143–147
3 ANDERSON, J.: 'Sequential decoding based on an error criterion', *IEEE Trans. Inform. Theory*, 1994, **40**, pp. 546–554
4 MARTIN, I., HONARY, B., and FARRELL, P.G.: 'Modified minimum weight decoding for Reed-Solomon codes', *Electron. Lett.*, 1995, **31**, pp. 713–714
5 OH, M., and SWEENEY, P.: 'Bit-level soft decision sequential decoding for RS codes',WCC'99, 1999, pp. 111–120
6 PEI, D., WANG, C., and OMURA, J.: 'Normal basis of finite field GF($2^m$)', *IEEE Trans. Inform. Theory*, 1986, **IT–32**, pp. 285–287
7 PERLIS, S.: 'Normal basis of cyclic fields of prime-power degree', *Duke Math. J.*, 1942, **9**, pp. 507–517
8 WOLF, J.K.: 'Efficient maximum likelihood decoding of linear block codes using a trellis', *IEEE Trans. Inform. Theory*, 1978, **IT–20**, pp. 76–78
9 PERTERSON, W., and WELDON, E.: 'Error-correcting code' (MA:MIT Press, 1972)
10 BERLEKAMP, E.: 'Algebraic coding theory' (MacGraw-Hill, New York, 1968)

## Bipolar/CMOS current-source flip-flop for application in neuro-fuzzy systems

T. Serrano-Gotarredona, B. Linares-Barranco and A.G. Andreou

A new current source flip-flop is presented which delivers an analogue current according to the state it stores. To enhance precision the output current is delivered while the main transistors are biased as CMOS compatible lateral bipolars. For reading and writing, these transistors are biased as regular MOS transistors. The resulting cell is extremely compact, allows low-voltage operation and is useful for neural and fuzzy based mixed mode processing systems.

*Introduction:* Computation of the $l_1$ norm of a vector stored in memory is a common task in neural and/or fuzzy based processing systems [1, 2]. Both functions, storage and computation, can be accomplished simultaneously by the use of a 'current-source flip-flop'. Such a circuit can be thought of as the simplest mixed-mode circuit since it simultaneously implements a 1 bit storage digital element (a flip-flop) and an analogue current source which is turned ON or OFF according to the state of the flip-flop.

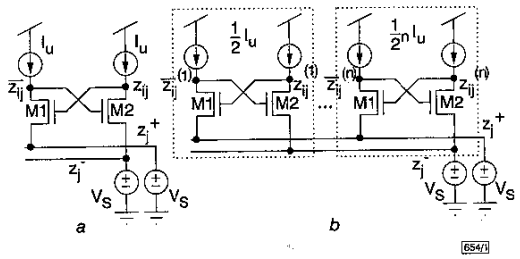


**Fig. 1** *Conceptual diagram of current source flip-flop*

*a* Current source flip-flop circuit
*b* Current source memory cell

*Current source flip-flop:* Fig. 1*a* shows the basic concept behind the current source flip-flop circuit. Two current sources of equal value $I_u$ are connected with two NMOS transistors $M1$ and $M2$ in a flip-flop configuration. The sources of the two NMOS transistors are connected to two lines tied to a fixed voltage $V_S$ by peripheral voltage sources. Depending on the state of the flip-flop the currents injected into these lines change: if $z_{ij} = 1$ the circuit injects a current $I_u$ into line $z_j^+$, while if $z_{ij} = 0$ the circuit injects current $I_u$ into line $z_j^-$. If $N$ of these current source flip-flops are connected horizontally sharing lines $z_j^+$ and $z_j^-$, the total current injected into line $z_j^+$ would be

$$I(z_j^+) = \sum_{i=1}^{N} z_{ij} I_u = I_u |\mathbf{z}_j| \qquad (1)$$

which is proportional to the $l_1$ norm of vector $\mathbf{z}_j \equiv (z_{1j}, ..., z_{Nj})$, stored in the $N$ flip-flops. All current source flip-flops in the same row can be set to '1' by momentarily lowering voltage $V_S$ for line $z_j^+$, or set to '0' by lowering the voltage at line $z_j^-$. Grouping $n$ current source flip-flops with binarily weighted current sources yields an $n$-bit current source memory cell. This is shown in Fig. 1*b*. In this case, the current injected into line $z_j^+$ would be

$$I(z_j^+) = I_u \sum_{l=1}^{n} z_{ij}^{(l)} \frac{1}{2^l} = I_u z_{ij} \qquad (2)$$

where $z_{ij}$ may take values between 0 and $1 - 1/2^n$ in steps of $1/2^n$. Connecting $N$ $n$-bit current source memory cells in a row sharing lines $z_j^+$ and $z_j^-$ enables the generation of

$$I(z_j^+) = I_u \sum_{i=1}^{N} z_{ij} = I_u |\mathbf{z}_j| \qquad (3)$$

where $\mathbf{z}_j$ is an $N$ component vector with each component represented by an $n$-bit digital word. The maximum number of bits $n$ is limited by how well the current sources match.

*Implementation of current sources:* Current sources $I_u$ or $I_u/2^i$ of Fig. 1 should be generated in such a way that mismatches in the reference value $I_u$ are as small as possible while not leading to too great an increase in chip area consumption. One possibility is to use CMOS compatible lateral bipolar transistors [3]. It is known that the mismatch behaviour for these transistors is much better than for equivalent MOS transistors (up to a factor of 10 improvement in standard deviation, depending on current level and technology) [4]. Fig. 2*a* shows the complete current source flip-flop operating in bipolar mode. Current sources with the same unit current $I_u$ (or $I_u/2^n$) are arranged by sharing the emitter terminal, while voltage $V_{base}$ is constant and common for all current-source flip-flops on the chip. Voltage $V_{emitter}$ is set at the periphery of the current-source flip-flop array by using the Serrano active-input current mirror principle [5, 6]. This current mirror is shown in Fig. 3*a* for transistors biased in bipolar mode and in Fig. 3*b* for transistors biased as MOS devices. At the periphery, current source $I_u/2^n$, the differential input amplifier and transistor $Q_{in}$ (or $M_{in}$) set the emitter (or source) voltage so that all transistors $Q_{o1} - Q_{oM}$ (or $M_{o1} - M_{oM}$) act as current sources of value $I_u/2^n$. The use of this current mirror enables the base (or $n$-well) terminal to be shared by all flip-flop current sources on the chip, thus allowing a very dense layout. Also, by simply rebiasing voltages $V_{base}$ and $V_{gate}$ for the whole chip, the current-source flip-flops switch between bipolar and MOS operation.

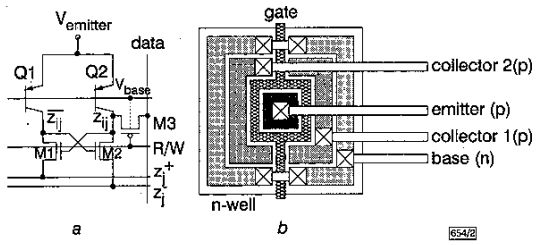


**Fig. 2** *Current source flip-flop operating in bipolar mode and physical layout of two-collector lateral bipolar pnp structure*

*a* Current source flip-flop with bipolar *pnp* transistors as current sources
*b* Physical layout of two-collector lateral bipolar *pnp* structure

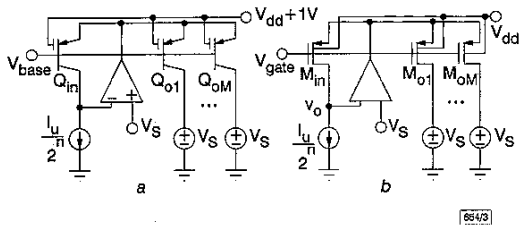


**Fig. 3** *Source/emitter driven p-type current mirrors*

*a* Bipolar transistor version
*b* MOS version

*Writing to flip-flop cells:* Flip-flops are reset all at the same time by controlling the values of $V_S$ for all lines, as mentioned earlier. The setting of a single flip-flop is carried out by biasing the current source transistors $Q_1$ and $Q_2$ in MOS mode and turning ON PMOS switch transistor $M_3$ by activating line '*R/W*', which connects node $z_{ij}$ to line 'data'. This cannot be activated while operating $Q_1$ and $Q_2$ in bipolar mode, because the $n$-well of $M_3$ is connected to $V_{base}$, which would forward bias the drain-bulk (*Data*-$V_{base}$) junction of $M_3$ when trying to write a '1' into $z_{ij}$. Lowering the high voltage at 'data' to avoid forward biasing of the junction would not make it possible to change the state of the flip-flop from '0' to '1'. A valid alternative would be to put $M_3$ into an independent $n$-well, at the cost of a high area penalty. Using an NMOS transistor for $M_3$ does not solve the problem either, because when 'data' is high $M_3$ would not have enough driving capability to switch the flip-flop state. Consequently, a valid and interesting alternative that allows writing operation, compact layout and precision bipolar operation, is to rebias $Q_1$ and $Q_2$ in MOS mode for writing. To switch back and forth between bipolar and MOS modes without losing the stored states (of all flip-flops on chip), the current sources should not be turned OFF. This is assured by applying the following biasing sequence:

(i) Starting with $Q_1$ and $Q_2$ in bipolar mode ($V_{base} = V_{DD} - 1$V, $V_{gate} = V_{DD} + 1$V), lower the gate voltage to approximately $V_{DD} - 1.5$V. This will turn ON the MOS mode without turning OFF the bipolar mode. Fig. 4*a* shows, for a single transistor, $I_{DS/CE}$ against $V_{DS/CE}$ with $V_{base} = V_{DD} - 1$V while changing $V_{gate}$ from $V_{DD} + 1$V to $V_{DD} - 1.5$V. Note that as both current driving mechanisms (bipolar and MOS) become active, the current increases.

(ii) Change $V_{base}$ from $V_{DD} - 1$V to $V_{DD}$. This will turn OFF the bipolar mode. Fig. 4*b* shows, for a single transistor, $I_{DS/CE}$ against $V_{DS/CE}$ with $V_{gate} = V_{DD} - 1.5$V while changing $V_{base}$ from $V_{DD} - 1$V to $V_{DD}$.

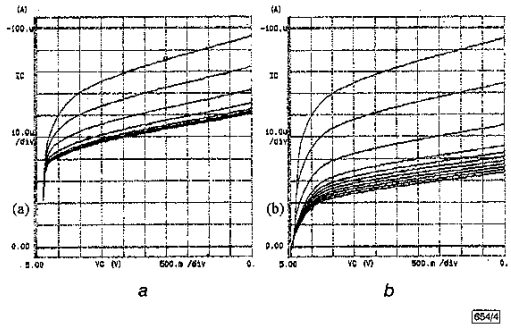


**Fig. 4** *Transistor current against $V_{DS/CE}$*

*a* $V_{base} = V_{DD} - 1$V and $V_{gate}$ changes from $V_{DD} + 1$V to $VDD - 1.5$V
*b* $V_{gate} = V_{DD} - 1.5$V and $V_{base}$ changes from $VDD - 1$V to $V_{DD}$

As can be seen, by following steps (i) and (ii) the transistors change from bipolar to MOS mode without stopping to drive current, and consequently without losing the flip-flop states. The same remains valid for the inverse operation. Consequently, for flip-flop writing, all flip-flops are changed from bipolar to MOS mode, the specific flip-flops to be altered are addressed and their states set appropriately. Afterwards, all flip-flops are switched back to bipolar mode.

A $125 \times 45$ array of these current-source flip-flops has been fabricated using the HP 0.5μm MOSIS CMOS process, as part of a neuro-fuzzy processing system, which occupies an area of $2.2 \times 2.2\text{mm}^2$. Each cell occupies an area of $22.4 \times 9.8\mu\text{m}^2$, with minimum size current source transistors $Q_1$ and $Q_2$. Operation of the current-source flip-flops has been verified for the current source ($I_u$) range between 1nA and 1μA. The complete neuro-fuzzy system is currently under test, and corresponding system level results will be reported in due course.

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**References**

1 SÁNCHEZ-SINENCIO, E., and LAU, C.: 'Artificial neural networks' (IEEE Press, 1995)
2 CARPENTER, G.A., and GROSSBERG, S.: 'Pattern recognition by self organizing neural networks' (MIT Press, Cambridge, MA, 1991)
3 ARREGUIT, X.: 'Compatible lateral bipolar transistors in CMOS technology: Model and applications'. PhD Thesis, Ecole Polytechnique Federale de Lausanne, 1989
4 PAN, T.W., and ABIDI, A.A.: 'A 50-dB variable gain amplifier using parasitic bipolar transistors in CMOS', *IEEE J. Solid-State Circuits*, 1989, **SC-24**, (4), pp. 951–961
5 SERRANO-GOTARREDONA, T., and LINARES-BARRANCO, B.: '7-decade tuning range CMOS OTA-C sinusoidal VCO', *Electron. Lett.*, 1998, **34**, (17), pp. 1621–1622
6 SERRANO-GOTARREDONA, T., LINARES-BARRANCO, B., and ANDREOU, A.G.: 'Very wide range tunable CMOS/bipolar current mirrors with voltage clamped input', to be published in *IEEE Trans. Circuits Syst. II*, 1999


## High Q active inductor with loss compensation by feedback network


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A novel high Q active inductor with loss compensation achieved using an active RC feedback network is proposed. This active RC feedback network yields a frequency-insensitive negative resistance that can compensate for the constant internal loss of active devices. Thus, a Q value of > 1000 can be obtained.


*Introduction:* A constant internal loss always exists in active devices due to several factors such as the conductance of the drain to source of an FET and DC bias circuits. This effect has been reported several times [1, 2]. Negative resistance has been used to achieve a high Q, but this can only be carried out in a narrow band [3]. The use of passive RC feedback networks in active inductor design has been proposed, but the Q factor is still relatively low [4, 5]. A passive feedback network is not sufficient for achieving loss compensation. If an active RC feedback network is integrated into the circuit, a constant negative resistance will result. This negative resistance will compensate for the devices' constant internal loss. Thus, the total loss will be much smaller and high Q can then be achieved.

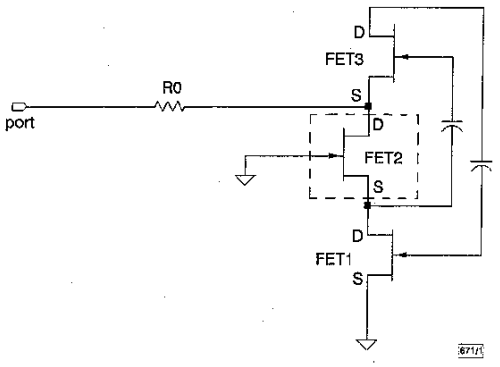


**Fig. 1** *Original circuit configuration of loss compensation active inductor*

Fig. 1 shows the original loss compensation technique circuit proposed by Hayashi *et al.* [6]. This circuit can only produce a very small inductance of ~0.5nH and works above 5GHz. For frequencies below 5GHz, the loss compensation circuit will lose its functionality.

In this Letter, a new circuit configuration which incorporates loss compensation by negative resistance is proposed. The resultant Q factor is very high and the circuit has a very good performance.

*Circuit configuration:* The proposed circuit is shown in Fig. 2. C1, C2, R1, R2 and FET2 form an active RC feedback network. C2 is used to increase the negative resistance value. C3 is adapted to increase the active inductance. Because the feedback active device (FET2) output is frequency dependent, a frequency-dependent negative resistance can easily be obtained. To reduce the frequency dispersion effect on the negative resistance, an RC network is added to FET2. The broadband characteristics of a nearly constant negative resistance can be achieved by adjusting C1, C2, R1 and R2. A resistor R0 is added in series with the circuit because the constant negative resistance is larger than the constant loss of the devices. If a proper value of R0 is chosen, a high Q broadband inductor can be realised.

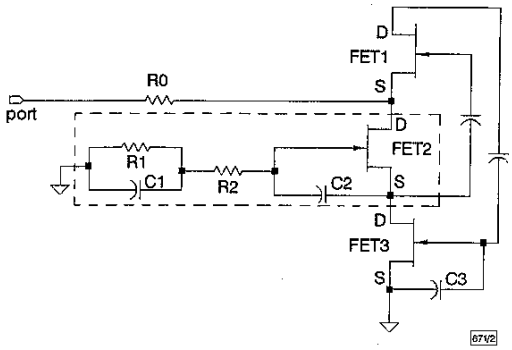


**Fig. 2** *Proposed active inductor with loss compensation by feedback network*

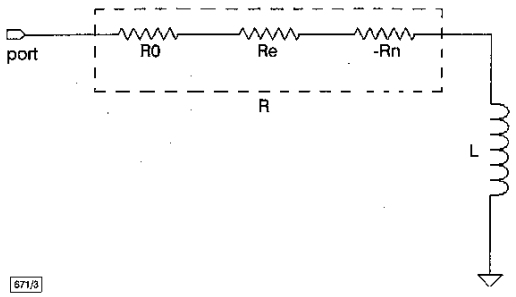


**Fig. 3** *Equivalent circuit of proposed active inductor*

The resultant equivalent circuit is depicted in Fig. 3. *Re* represents the constant loss of active devices, *Rn* the equivalent constant negative resistance and *L* the equivalent active inductance.

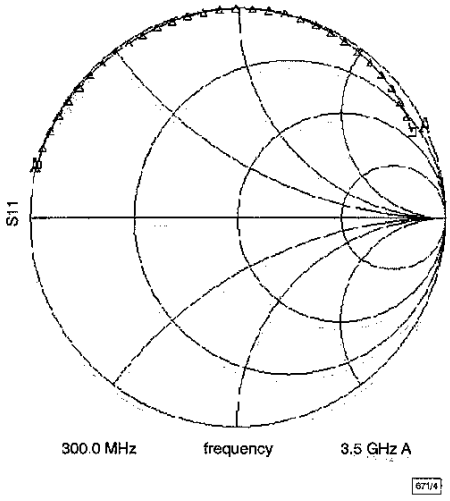


**Fig. 4** *Microwave performance of proposed active inductor*

*Simulation and results:* All simulations were carried out using HP-MDS. Avantek-106501ns, biased at 3V, 10mA, were employed as the active devices. In the circuit, the components values were $R0$ = 27.8Ω, $R1$ = 48Ω, $R2$ = 113 Ω, $C1$ = 0.4pF, $C2$ = 0.04pF, $C3$ =