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Current-mode fully-programmable piece-wise-linear block for neuro-fuzzy applications

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A new method to implement an arbitrary piece-wise-linear characteristic in current mode is presented. Each of the breaking points and each slope is separately controllable. As an example a block that implements an N-shaped piece-wise-linearity has been designed. The N-shaped block operates in the subthreshold region and uses only ten transistors. These characteristics make it especially suitable for large arrays of neuro-fuzzy systems where the number of transistors and power consumption per cell is an important concern. A prototype of this block has been fabricated in a 0.35 μm CMOS technology. The functionality and programmability of this circuit has been verified through experimental results.

Introduction: A piece-wise-linear element is commonly required to implement the activation function of neural systems and the membership function in the case of fuzzy systems [1]. In most cases, complete programmability of the breaking points and slopes of the different pieces of the nonlinearity is desirable. Normally, it is necessary to implement an activation (or membership) function per neural (or fuzzy) cell. The large number of cells integrated in VLSI neural and fuzzy systems make the simplicity (in transistor number) and power consumption of the piece-wise-linear block important concerns.

In the following Section, a new method to implement a current-mode piece-wise-linear characteristics is presented. A block implementing an N-shaped piece-wise-linearity is then introduced. The block requires only ten transistors per cell and can be operated at very wide current ranges. A small prototype has been fabricated in a CMOS 0.35 μm technology. Experimental results are provided.

Current-mode piece-wise-linear block: Any arbitrary unidimensional piece-wise-linear function $f(u)$ can always be decomposed as the sum of one-sided rectified functions:

$$f(u) = \sum_i (\pm m_i[\pm(u - u_i)]^+) \quad (1)$$

where $[x]^+$ denotes the one-sided rectification operator (x if $x \geq 0$ or 0 if $x \leq 0$), m_i is the slope of the gain segment and u_i is its breaking point. Fig. 1*a* shows the four possible one-sided rectified functions which correspond to the two possible signs of the slope and the two possible signs of the output function. Each sub-figure in Fig. 1*b* shows a proposed current-mode circuit block that implements each of the functions in Fig. 1*a*. The transistors in Fig. 1*b* are intended to operate in the subthreshold region. This way, the slopes m_i of the gain segments can be controlled through the bias voltages V_{ia} and V_{ib}. In particular,

$$m_i = \exp\left(\frac{V_{ia} - V_{ib}}{nU_T}\right) \quad (2)$$

where n is the slope factor of the MOS transistors (NMOS n_n or PMOS n_p) in the subthreshold region [2]. However, the large variability of the slope factors (n_n, n_p) and the transistor threshold voltages (V_{Tn}, V_{Tp}) from run to run, makes it impractical to control the m_i slopes by controlling directly the voltage biases. This inconvenience can be solved using current biases to control the slopes. Fig. 2 shows the NMOS and PMOS versions of the biasing blocks. The current references u_{ref} and $m_i u_{ref}$ are used to set the appropriate values of the voltages V_{ia} and V_{ib}, such that the ratio between the currents flowing through the two branches is m_i. In a large neural or fuzzy system, the biasing blocks are common to all the cells in the chip. The amplifiers in Fig. 2 must deliver sufficient current to all the output branches in the different cells. This means that the output stage of the amplifiers must be scaled with the number of cells in the chip.

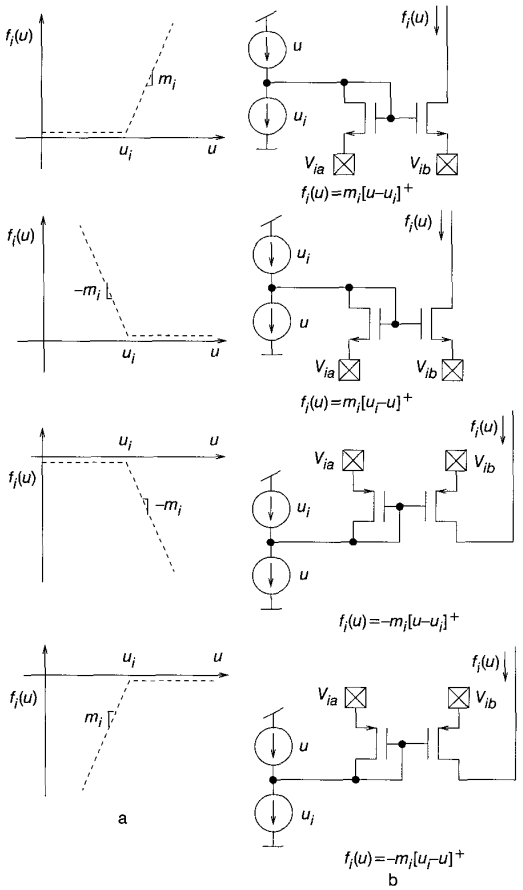

Fig. 1 *Functions and implementations*
a Four possible one-sided rectified functions
b Schematic of four implementations

In our application, we needed to synthesise an N-shaped PWL function such as that shown in Fig. 3, which is a block commonly used as the activation function in neural networks implementations. The block must be adaptive, i.e. we want to control independently the two breaking points u_1, u_2 and the three slopes m_0, m_1 and m_2. As shown in Fig. 3, the PWL function $f(u)$ can be decomposed as the sum of three components, named as $f_0(u)$, $f_1(u)$ and $f_2(u)$ in Fig. 3. Fig. 4 shows the schematics of the current-mode block synthesised using our general method explained so far. The proposed method is generic for any piece-

wise-linear function (for finite m_i), and is consequently applicable to any neuro-fuzzy nonlinear function.

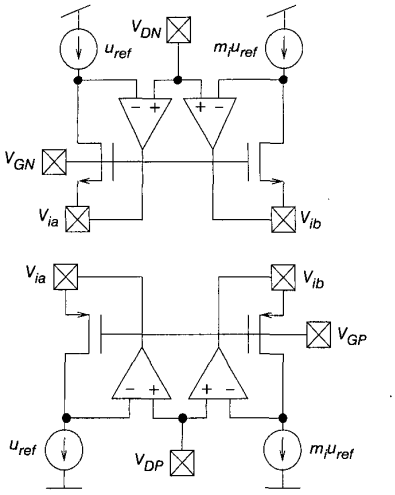

Fig. 2 *Biasing blocks that generate voltage biases V_{ia} and V_{ib} from reference currents I_{REF} and m_iI_{REF}*

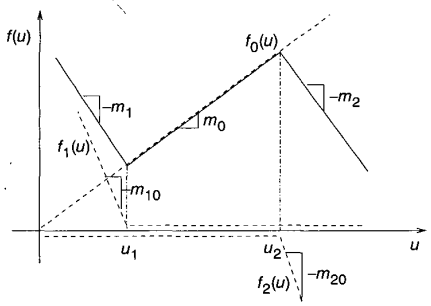

Fig. 3 *N-shaped piece-wise-linear function*

Experimental results: The piece-wise-linear block in Fig. 4 has been designed and fabricated in a 0.35 μm CMOS technology provided by the AMS foundry.

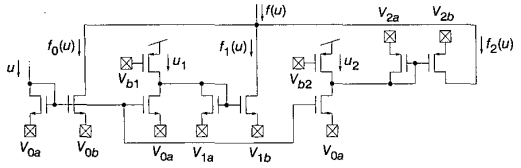

Fig. 4 *Schematics of current-mode N-shaped piece-wise-linear block*

Seven biasing currents are used to control the breaking points and slopes. Currents u_1 and u_2 set the two breaking points. The central slope m_0 is controlled by the ratio of two currents $m_0u_{ref\,0}/u_{ref\,0}$. Slope m_{10} is set by $m_{10}u_{ref\,0}/u_{ref\,0}$ and slope m_{20} is given by $m_{20}u_{ref\,2}/u_{ref\,2}$. All the biasing currents are derived from the same reference current I_{REF} through five-bit DAC converters. The value of each current can be varied between $\{0, I_{REF}/16, \ldots, 2I_{REF}\}$. The functionality of the block has been verified for at least four decades of variation of the working currents. The block works correctly for a reference current varying from $I_{REF} = 50$ pA to $I_{REF} = 500$ nA.

Fig. 5*a* shows the controllability of the central slope m_0. In the measurements of Fig. 5*a* $I_{REF} = 5$ nA, $u_1 = 10I_{REF}/16$, $u_2 = 25I_{REF}/16$, $u_{ref\,0} = 10I_{REF}/16$, $u_{ref\,2} = 10I_{REF}/16$, while $m_0u_{ref\,0}$ is varied for 0 to $22I_{REF}/16$. The values of $m_{10}u_{ref\,0}$ and $m_{20}u_{ref\,2}$ are simultaneously swept from $10I_{REF}/16$ to $32I_{REF}/16$ so that, as can be observed, the m_1 and m_2 slopes remain constant and approximately equal to 1.

Fig. 5*b* shows the programmability of the m_2 slope. In these curves, $u_1 = 10I_{REF}/16$, $u_2 = 25I_{REF}/16$, $u_{ref\,0} = 10I_{REF}/16$, $u_{ref\,2} = 10I_{REF}/16$, $m_0u_{ref\,0} = 10I_{REF}/16$, $m_{10}u_{ref\,0} = 20I_{REF}/16$ and $I_{REF} = 5$ nA, while $m_{20}u_{ref\,2}$ is varied from 0 to $2I_{REF}$.

The controllability of the breaking point u_2 is demonstrated in the measurements of Fig. 5*c*. In the curves of Fig. 5*c*, $u_1 = 10I_{REF}/16$, $u_{ref\,0} = 10I_{REF}/16$, $u_{ref\,2} = 10I_{REF}/16$, $m_0u_{ref\,0} = 10I_{REF}/16$, $m_{10}u_{ref\,0} = 19I_{REF}/16$, $m_{20}u_{ref\,2} = 19I_{REF}/16$, $I_{REF} = 5$ nA, and u_2 varies from $11I_{REF}/16$ to $2I_{REF}$.

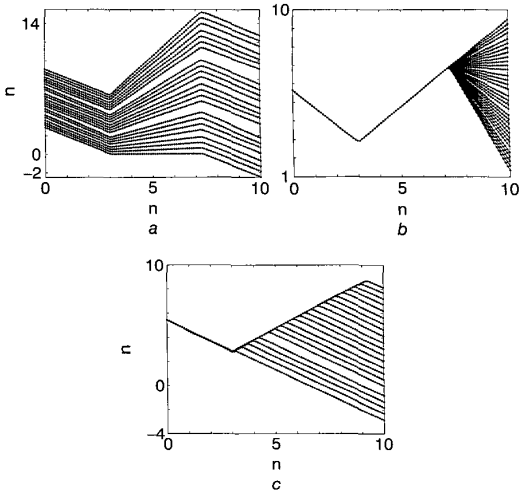

Fig. 5 *Measured input–output characteristics*

a For different values of central slope m_0
b For different values of m_2 slope
c For different values of u_2 breaking point

Conclusions: We have proposed a new methodology to implement arbitrary piece-wise-linear functions in current mode. The breaking points and the slopes of the pieces of the nonlinearity are separately programmable. The transistors operate in the subthreshold regime, with currents well below the micro ampere, what makes this block especially suitable for large neural or fuzzy systems with low-power consumption. As an example, we have designed an N-shaped piece-wise-linearity with two breaking points and three independently controllable slopes. The correct operation of the block has been verified experimentally. To our knowledge, a piece-wise-linear function with such a range of parameter variation and operating current range has not been previously published in the literature.

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