MOS/Bipolar active Input Current Mirrors with 13-Decades Gain Adjustment Range

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Abstract

This paper introduces two new active input current mirror topologies. They present the following advantages with respect to the conventional active input current mirror: (a) one of them does not require stability compensation while the other may require under some circumstances, (b) once they are stable for a given input current level, their input current can be made arbitrarily small, (c) the current mirror gain can be controlled continuously through a gate voltage for a range of 13-decades according to our experimental results, and (d) the circuit can be operated by either biasing the mirroring transistors as MOS or as lateral bipolar devices. One of the current mirrors has been used to build a constant input range OTA whose transconductance can be tuned over 7 decades. This OTA is then used to assemble a g_m-C sinusoidal VCO whose frequency can be tuned from 74mHz to 1MHz. To our knowledge this has never been achieved before using g_m-C MOS oscillators.

1. Introduction

The conventional active input current mirror [1], shown in Fig. 1(a), is a current mirror that clamps its input node voltage. This is advantageous for achieving high precision current replication or to decrease the delay due to charge and discharge of its input node parasitic capacitance C_p. This current mirror suffers, however, from an important drawback: once compensated, its input current cannot be made arbitrarily small. To see this, let us redraw its input stage as shown in Fig. 1(b), which is a two stage opamp [2] in unity gain feedback configuration. Fig. 1(c) shows its small signal equivalent circuit, where g_{ma}, g_{oa} and C_{pa} model a single pole behavior for the differential input voltage amplifier, g_{m1} and g_{o1} model transistor $M1$ and the current source I_{in} output conductance and C_c represents the drain to gate $M1$ capacitance in parallel with an eventual compensation capacitor. This circuit yields a second order system whose stability condition is

$$g_{oa}(C_p + C_c) + g_{o1}(C_{pa} + C_c) + C_c(g_{m1} - g_{ma}) > 0 \quad (1)$$

The third term in eq. (1) is dominant. If I_{in} (and therefore, g_{m1}) is made arbitrarily small, unstability results. In this paper we present two new active input current mirror topologies which do not present this problem. This allows to use the mirrors for a very wide range of input currents (over six decades). Furthermore, the mirror gain can be adjusted continuously over many decades through a gate voltage. Even more, the mirrors can be made to operate as well by biasing the mirroring transistors as CMOS compatible lateral bipolar devices.

2. Two new active-input current mirrors

The circuit in Fig. 2(a) is a source driven active input current mirror where gate voltage of input and output mirroring transistors is connected to a fixed bias voltage. For the differential input voltage amplifier a simple OTA can be used. The OTA must be able to provide twice the maximum input current. To analyze stability behavior the mirror input stage can be redrawn like in Fig. 2(b) as a special two stage opamp in unity gain feedback. As opposed to Fig. 1(b), first stage is inverting while second stage is not. By simulation and experimentally, it can be verified that this structure might become unstable. This can be predicted by assuming a second order model for the OTA. Fig. 2(c) shows the small signal equivalent circuit of that in Fig. 2(b) where $g_m(s) = g_{ma}(1 - s/\omega_a)$ and ω_a models the delay introduced by the OTA internal nodes [3]. If the OTA is compensated ($C_{pa} > g_{ma}/\omega_a$) stability is guaranteed if

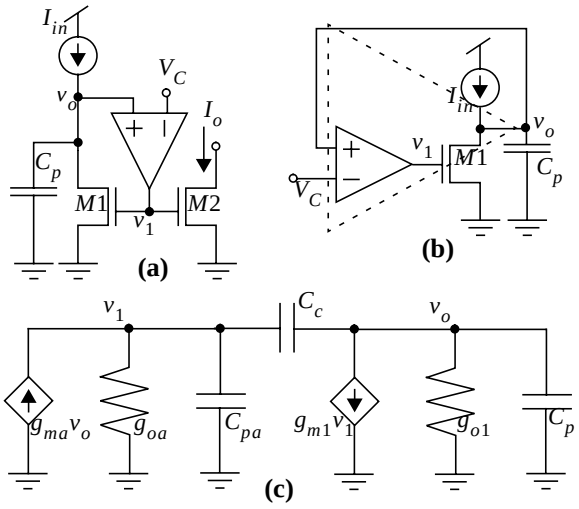

Fig. 1: Conventional Active-Input Current Mirror, (a) schematic, (b) input stage drawn as 2-stage opamp, (c) small signal equivalent circuit

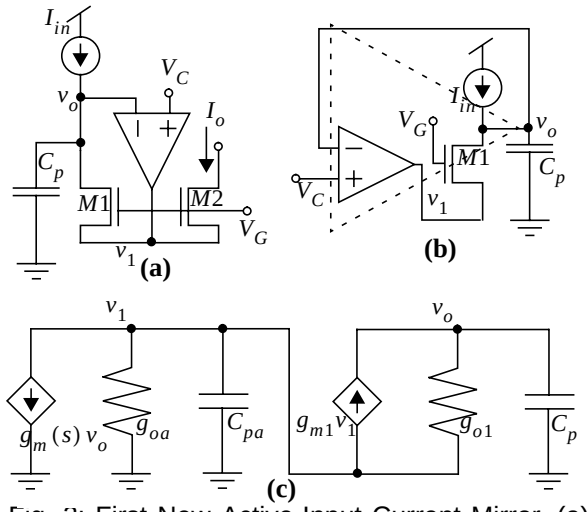

Fig. 2: First New Active-Input Current Mirror, (a) schematic, (b) input stage drawn as 2-stage opamp, (c) small signal equivalent circuit

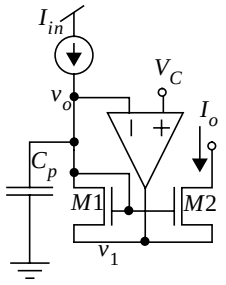

Fig. 3: Second New Active-Input Current Mirror

$$C_p > \frac{g_{ma} g_{m1}}{\omega_a (g_{oa} + g_{m1})} \tag{2}$$

If this condition cannot be satisfied, a compensation capacitor C_A can be added between nodes v_1 and v_o, and the stability condition changes to

$$C_A > g_{m1}\left(\frac{1}{\omega_a} - \frac{C_p}{g_{ma}}\right) - C_p \frac{g_{oa} + g_{o1}}{g_{ma}} \tag{3}$$

Eqs. (2)-(3) are increasing functions of g_{m1} and I_{in} (If eq. (2) is not satisfied then the right hand side of eq. (3) is positive). Therefore, if the circuit is stable for the maximum g_{m1} (and I_{in}) value, it remains stable for any smaller value. Note that $M2$ also takes current from the OTA and consequently changes the circuit in Fig. 2(c). Also the load connected at the drain of $M2$ changes this circuit. However, it is not difficult to show that eqs. (2)-(3) remain valid under these circumstances.

Fig. 3 shows an alternative source driven active input current mirror. In this case $M1$ is connected as a diode in the OTA negative feedback loop. Therefore, if the OTA is compensated, this circuit is stable because $M1$ is here a passive device.

3. Transient response

Assuming the voltage amplifier settles instantly, the large signal transient response of the circuit in Fig. 2(b) can be computed. The current through transistor $M1$ in subthreshold is

$$I_{M1} = I_{s1}' e^{\frac{\kappa (V_G - v_1)}{U_T}} = I_{s1} e^{-\frac{\kappa v_1}{U_T}} \tag{4}$$

where κ and I_{s1}' are positive technology dependent parameters. Source voltage v_1 is given by $v_1 = A_V (V_C - v_o)$, where A_v is the amplifier gain. Since $I_{in} = I_{M1} + C_p \dot{v}_o$ and

$$v_o = V_C - \frac{v_1}{A_v} = V_C + \frac{U_T}{A_v \kappa} \ln \frac{I_{M1}}{I_{s1}} \tag{5}$$

the following time domain nonlinear first order differential equation results

$$I_{in} = I_{M1} + C_p \frac{U_T \dot{I}_{M1}}{A_v \kappa I_{M1}} \tag{6}$$

whose solution, for constant I_{in} is

$$I_{M1}(t) = \frac{I_{M1}(0)\, I_{in}}{(I_{in} - I_{M1}(0))\, e^{-(A_v \kappa I_{in}/U_T C_p)\, t} + I_{M1}(0)} \tag{7}$$

Therefore, if I_{in} changes in a step fashion from rI_c to I_c then in eq. (7) $I_{in} = I_c$ and $I_{M1}(0) = rI_c$. The time delay t_d necessary for I_{M1} to reach RI_c is then

$$t_d = \tau \ln \frac{1/r - 1}{1/R - 1} \quad , \quad \tau = \frac{U_T C_p}{A_v \kappa I_c} \tag{8}$$

If A_v is sufficiently large τ can be made reasonably small, even for low values of I_c. For high values of I_c the delay will be dominated by the differential amplifier and will tend to be independent on I_c. For the circuit in Fig. 3 a similar analysis can be performed. The resulting equations are equal to eqs. (7)-(8), except that A_v is substituted by $A_v + 1$.

4. Continuously adjustable gain

For the mirrors in Fig. 2(a) and Fig. 3, if transistors $M1$ and $M2$ are operated in weak inversion, and if the gate of transistor $M2$ is connected to an independent bias voltage V_{G2}, then current mirrors with continuously adjustable gain (through V_{G2}) result. Currents through $M1$ and $M2$ are

$$\left.\begin{aligned} I_{in} &= I_{s1} e^{\frac{V_G - v_1}{U_T}} \\ I_o &= I_{s2} e^{\frac{V_{G2} - v_1}{U_T}} \end{aligned}\right\} \Rightarrow I_o = A_I I_{in} \;,\; A_I = \frac{I_{s2}}{I_{s1}} e^{\frac{V_{G2} - V_G}{U_T}} \tag{9}$$

where U_T is thermal voltage, I_{s1} and I_{s2} are positive parameters, and the current mirror gain A_I is controlled by $V_{G2} - V_G$. For the circuit of Fig. 2(a) voltage V_G is an independent bias, while for the circuit of Fig. 3 $V_G = V_C$.

5. CMOS compatible lateral bipolar mode

The structure of Fig. 2(a) can be directly used in bipolar mode [4] if the CMOS process is p-well (if process is n-well the same discussion applies for mirrors with p-transistors). The gates of $M1$ and $M2$ need to be biased around $1V$ below ground (or $1V$ above power supply for the p-version), and the *Base* (or well) voltages need to be sufficiently high so that the *Base-Emitter*

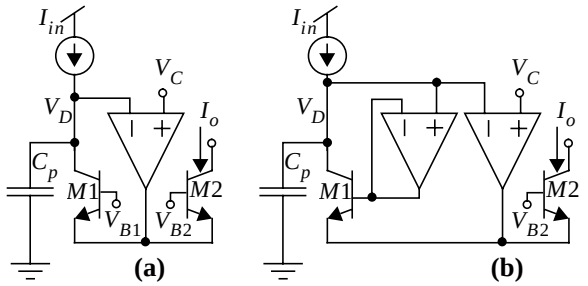

Fig. 4: Bipolar versions of continuously adjustable gain current mirrors, (a) for the case of Fig. 2(a), and (b) for the case of Fig. 3.

junctions can be forward biased. Fig. 4(a) shows the bias arrangement to operate the circuit of Fig. 2(a) in bipolar mode and with continuously adjustable gain. For the circuit of Fig. 3 not only re-wiring is necessary, but also the addition of an extra voltage buffer if one is not willing to neglect the extra *Base* current(s). The resulting circuit is shown in Fig. 4(b).

6. Experimental results

A set of current mirror prototypes have been fabricated in a 1.2μm n-well CMOS process. Transistors were laid out as square waffle structures with $L = 4.8\mu m$ and $W = 1378\mu m$. Fig. 5 shows measurements of I_o vs. I_{in}, for different gains, for an NMOS, a PMOS, and a lateral bipolar pnp mirrors. Input current was swept between $1pA$ and $1mA$. Gain control voltage (V_{G2} or V_{B2}) was swept with $50mV$ steps around V_{G1} or V_{B1}. In these log-log representations, lines of slope '1' represent a linear relationship between input and output, while position accounts for the gain. Circles denote the 1% linearity error region limits. For these regions the maximum and minimum current mirror gains are given in Table 1 as A_{min} and A_{max}. Also shown in Fig. 5 are the maximum size rectangles that could be drawn inside the 1% linearity error regions. Maximum and minimum current and gains for these boxes are given in Table 2. Note that in Fig. 5, for the unity gain curves, the 1% error interval is significantly larger than for the other curves. These limits are given in Table 1 under I_{min} and I_{max}.

The mirror in Fig. 2(a) was used to design the OTA shown in Fig. 6. By maintaining constant I_{ss} its linear

Table 1

Table 1	Absolute		Unity Gain	
	A_{min}	A_{max}	I_{min}	I_{max}
NMOS	2.7×10^{-8}	5.1×10^{5}	8.4×10^{-10}	9.3×10^{-5}
PMOS	2.1×10^{-8}	2.6×10^{6}	2.1×10^{-10}	1.3×10^{-4}
Bipolar	6.1×10^{-7}	1.2×10^{7}	2.1×10^{-10}	6.3×10^{-4}

Table 2

Table 2	I_{in}^{min}	I_{in}^{max}	I_{out}^{min}	I_{out}^{max}	A_{min}	A_{max}
NMOS	$1.0nA$	$630nA$	$69pA$	$0.94\mu A$	70μ	$1.0k$
PMOS	$0.22nA$	$89nA$	$4.4pA$	$0.19\mu A$	54μ	$0.7k$
Bipolar	$0.27nA$	$870nA$	$92pA$	$0.61\mu A$	77μ	$1.9k$

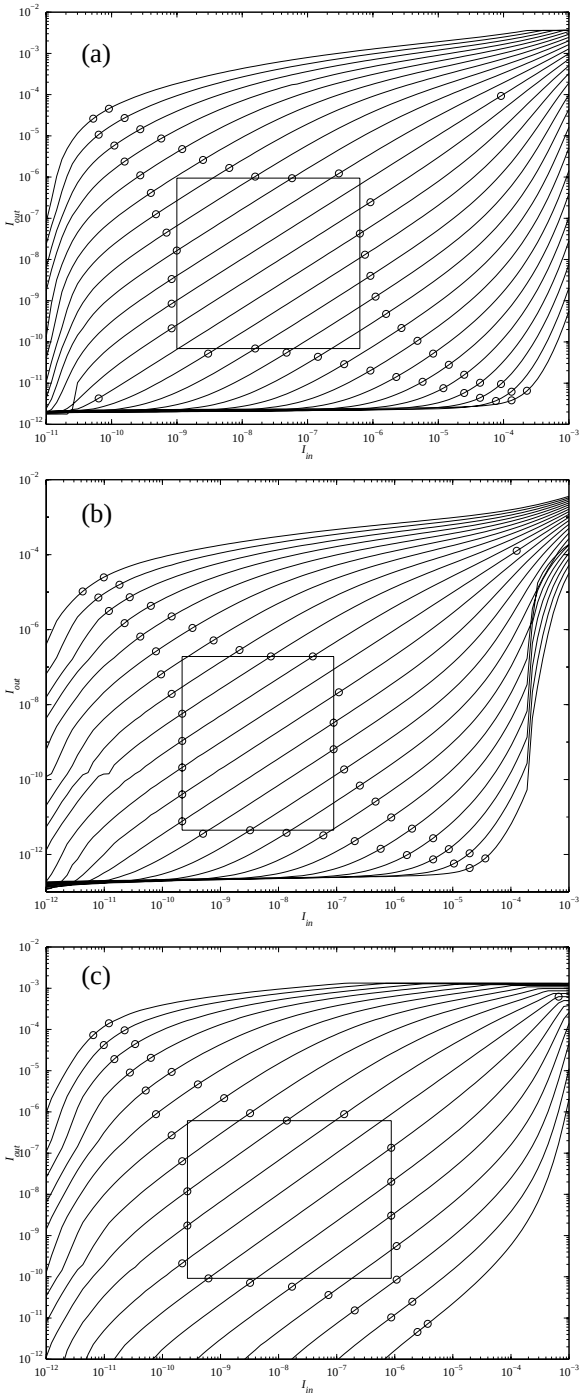

Fig. 5: Experimentally measured Output vs. Input Currents, for different gains, for (a) the NMOS mirror, (b) the PMOS mirror, and (c) the Bipolar mirror versions.

input range is not degraded. Its transconductance can be tuned through V_{G2} over many decades.

This OTA was then used in the g_m-C sinusoidal quadrature VCO shown in Fig. 7 [3]. Transconductances g_{mo} were tuned simultaneously through their V_{G2} control voltage to adjust the frequency of the VCO. Frequency could be tuned between $73.96mHz$ and $1.015MHz$ (over 7 decades). Fig. 8 shows the measured waveforms for the lowest and highest frequencies.

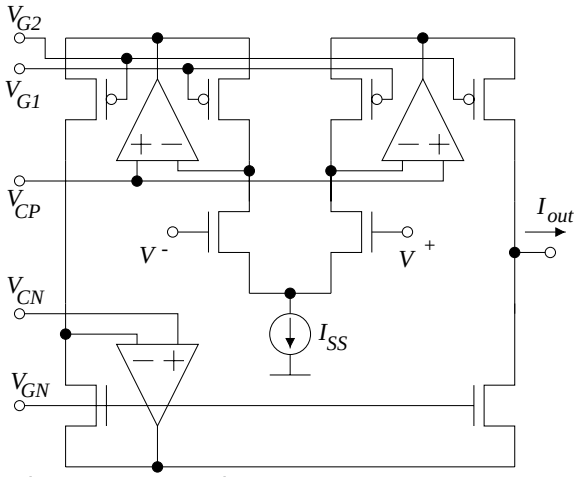

Fig. 6: Constant Linear Input Range OTA

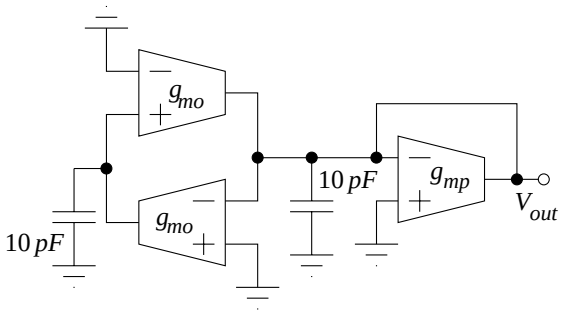

Fig. 7: Sinusoidal Quadrature g_m-C VCO

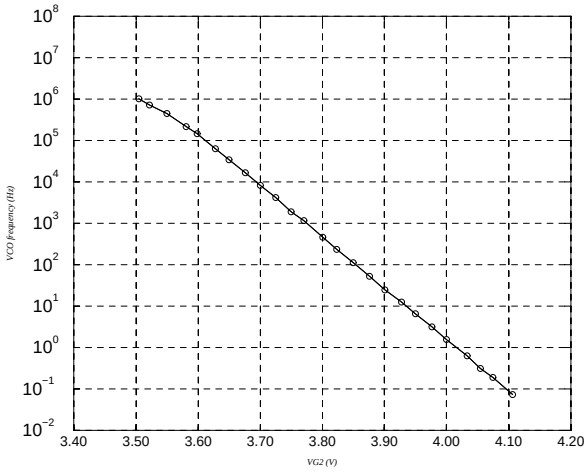

Fig. 9: Experimentally Measured Relationship between VCO frequency and V_{G2}

Finally, Fig. 9 depicts the meausred relationship between VCO frequency and control voltage V_{G2}.

7. Conclusions

Two new active-input current mirror structures are introduced. The novelty resides in that the active amplifier drives transistor sources instead of gates. This allows the amplifier to be connected in a negative

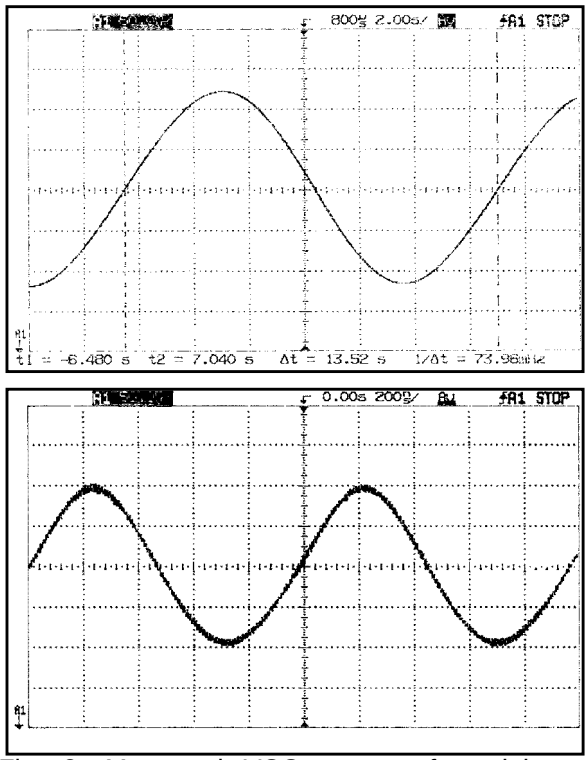

Fig. 8: Measured VCO outputs for minimum (73.94*mHz*) and maximum (1.015*MHz*) frequencies. Vertical scale is 50*mV/div* and horizontal scales are 2*s/div* for top trace and 200*ns/div* for bottom trace.

feedback loop configuration, instead of positive, which results in no need for compensation circuitry. Experimental measurements reveal that the structures are stable for currents varying over 9 decades. The gain of these current mirrors can be continuously tuned over 13 decades (while maintaining 1% linearity error in the mirroring operation). The mirrors can be used either with MOS transistors or with CMOS compatible lateral bipolar transistors. As an application example a constant linear input range OTA was designed, whose transconductance can be tuned over many decades. This OTA was used in a g_m-C sinusoidal VCO whose frequency could be tuned over 7 decades. Experimental results have been provided.

8. References

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