

A 5-Parameter Mismatch Model for Short Channel MOS Transistors

Teresa Serrano-Gotarredona and Bernabé Linares-Barranco

National Microelectronics Center

Ed. CICA Av. Reina Mercedes s/n, 41012 Sevilla Spain

E-mail: bernabe@imse.cnm.es

Abstract

A new 5-parameter MOS transistor mismatch model is introduced capable of predicting transistor mismatch with very high accuracy for ohmic and saturation strong inversion regions, including short channel transistors. The new model is based on splitting the contribution of the mobility degradation parameter mismatch into two components, and modulating them as the transistor transitions from ohmic to saturation regions. The model is tested for a wide range of transistor sizes (30), and shows excellent precision, never reported before for such a wide range of transistor sizes, including short channel transistors.

1. Introduction

Characterization and simulation of MOS transistor mismatch is crucial for precision analog design. Usually, statistical characterization parameters are extracted independently for different regions of operation [1],[2]. This works satisfactorily for square and long channel transistors, but when aspect ratios differ significantly or very small transistor lengths are used, the traditional mismatch models provide poor fit between measured and predicted values. In this contribution we report on an extended mismatch model whose statistical parameters are extracted simultaneously from curves measured in the ohmic and saturation regions. As a result an extraordinary fit between measured and predicted mismatch is obtained, for both regions of operation, and for a very wide range of transistor sizes, including minimum channel length transistors.

2. The New Mismatch Model

An acceptable strong inversion large signal transistor model for mismatch is [1]-[2],

$$I_{DS} = \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS_{eff}}}{1 + \theta(V_{GS} - V_T(V_{SB}))} V_{DS_{eff}} \quad (1)$$

$$V_T(V_{SB}) = V_{T0} + \gamma[\sqrt{\phi + V_{SB}} - \sqrt{\phi}] \quad (2)$$

where $V_{DS_{eff}} = V_{DS}$ for ohmic region ($V_{DS} \leq V_{GS} - V_T$) or $V_{DS_{eff}} = V_{GS} - V_T(V_{SB})$ for saturation ($V_{DS} \geq V_{GS} - V_T$), $\beta = \mu C_{ox} W/L$ is the current gain factor, V_{T0} is the zero-bias threshold voltage, γ is the bulk threshold parameter, and θ is the mobility degradation parameter. Assuming $\Delta\beta$, ΔV_{T0} , $\Delta\gamma$ and $\Delta\theta$ are the dominant transistor mismatch parameters

[1]-[2], differentiating eq. (1) yields the following current mismatch model for a given transistor pair

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_T} \left(\Delta V_{T0} + \frac{\partial V_T}{\partial \gamma} \Delta\gamma \right) + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta} \Delta\theta \quad (3)$$

where the set of four mismatch parameters $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\gamma, \Delta\theta\}$ would characterize this transistor pair mismatch for any bias point. However, for short channel transistors the effect of source and drain series resistance as well as carriers velocity saturation are important for mismatch, but are not modeled in eq. (1). The effect of drain and source series resistances can be included in eq. (1) by replacing V_{GS} by $V_{GS} - I_{DS}R_S$ and V_{DS} by $V_{DS} - I_{DS}(R_S + R_D)$. After neglecting high order terms an equation similar to eq. (1) results in which θ has been substituted by θ_{eff} ,

$$I_{DS} = \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS_{eff}}}{1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))} V_{DS_{eff}} \quad (4)$$

with

$$\theta_{eff} \approx \theta + \beta(R_S + R_D) - \beta R_D \frac{V_{DS_{eff}}}{V_{GS} - V_T} \quad (5)$$

Carriers velocity saturation v_s can be introduced by dividing the right hand side of eq. (1) by $1 + V_{DS_{eff}} \mu / (2v_s L)$ [3]-[4],

$$I_{DS} = \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS_{eff}}}{[1 + \theta_{eff}(V_{GS} - V_T)] \left[1 + \frac{\mu V_{DS_{eff}}}{2v_s L} \right]} V_{DS_{eff}} \approx \quad (6)$$

$$\approx \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS_{eff}}}{1 + \theta_{eff}(V_{GS} - V_T)} V_{DS_{eff}}$$

where,

$$\theta_{eff} \approx \theta + \beta(R_D + R_S) + \left(\frac{\mu}{2v_s L} - \beta R_D \right) \frac{V_{DS_{eff}}}{V_{GS} - V_T} \quad (7)$$

and both effects, series resistances and carriers velocity saturation, are included. Eq. (7) yields the following mismatch for $\Delta\theta_{eff}$

$$\Delta\theta_{eff} = \Delta\theta_o + \frac{V_{DS_{eff}}}{V_{GS} - V_T} \Delta\theta_e \quad (8)$$

where $\Delta\theta_o$ is the $\Delta\theta_{eff}$ mismatch in ohmic region for $V_{DS} \approx 0$ and $\Delta\theta_o + \Delta\theta_e$ is the mismatch in saturation, with

$$\Delta\theta_o = \Delta\theta + \Delta\beta(R_D + R_S) + \beta(\Delta R_D + \Delta R_S)$$

$$\Delta\theta_e = \frac{\Delta\mu}{2v_s L} - \frac{\mu}{2v_s L} \left[\frac{\Delta v_s}{v_s} + \frac{\Delta L}{L} \right] - R_D \Delta\beta - \beta \Delta R_D \quad (9)$$

In order to characterize the five mismatch parameters $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\gamma, \Delta\theta_o, \Delta\theta_e\}$, eq. (3) needs to be measured in ohmic (with $V_{DS} \approx 0$) while extracting mismatch parameters of eq. (3) with $\Delta\theta = \Delta\theta_o$, and in saturation while extracting mismatch parameters of eq. (3) with $\Delta\theta = \Delta\theta_o + \Delta\theta_e$.

3. Mismatch Parameter Extraction

A mismatch characterization chip including 30 different NMOS and PMOS transistor arrays of different sizes was fabricated in the ES2 1.0 μm CMOS process [6]-[7]. Transistor widths were $W = 40\mu m, 20\mu m, 10\mu m, 5\mu m, 2.5\mu m, 1.25\mu m$ while lengths were $L = 40\mu m, 10\mu m, 4\mu m, 2\mu m, 1\mu m$. Each array contained 30 transistor pairs. For each pair four I - V curves were measured:

Curve 1 (ohmic): $V_{DS}=0.1V, V_{SB}=0V, V_{GS} \in [1.5, 5V]$

Curve 2 (ohmic): $V_{DS}=0.1V, V_{GS}=3V, V_{SB} \in [0, 2V]$

Curve 3 (saturation): $V_{DS}=4V, V_{SB}=0V, V_{GS} \in [1.5, 5V]$ (10)

Curve 4 (saturation): $V_{DS}=4V, V_{GS}=3V, V_{SB} \in [0, 2V]$

First, using eqs. (1)-(2) the large signal parameters $\beta, V_{T0}, \gamma, \theta$ and ϕ were extracted from these curves for each transistor pair using nonlinear multi-parameters curve fitting techniques, such as the Levenberg-Marquadt method [5]. These parameters were used to compute the partial derivatives in eq. (3) for each of the four measured curves. Afterwards, four versions of eq. (3) were obtained, one for each of the curves in eqs. (10), and were fitted simultaneously to the measured data $\Delta I_{DS}/I_{DS}$ resulting in a unique set of mismatch parameters for each transistor pair $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\gamma, \Delta\theta_o, \Delta\theta_e\}$ valid for saturation and ohmic regions.

The precision with which the *mismatch parameters* are extracted depends on the number of data points measured for each curve, and on the precision with which each data point is measured. We noticed that using a large number of data points does not improve much the precision of the extracted parameters, and observed that a reasonable compromise between measurement-time and precision was obtained for 11 data points. On the contrary, it was very important to measure each data point with as much precision as possible, i.e. with as little measurement noise as possible. Instruments eliminate noise by repeating the measurement several times and providing the average as the result. In our case, we set the instrument to average 256 measurements. This way, when computing $\Delta I_{DS}/I_{DS}$, we did not obtain pure noise.

Regarding the large signal model, note that eqs. (6) and (2) describe a very simplistic MOS transistor model. This means that we cannot expect to obtain for all transistor sizes the same large signal parameters. Furthermore, for the same transistor, we should not expect to obtain the same *large signal parameters* when it is biased in ohmic or in saturation. Consequently, for each transistor, the large signal parameters should be extracted independently for Curves 1-2 and Curves 3-4.

For each transistor pair, the measurement/extraction procedure is as follows.

- 1) Measure Curve 1 for both transistors. Extract the *large signal parameters* $\{\beta, V_{T0}, \theta_{eff}\}_{ohmic}$.
- 2) Measure Curve 2 for both transistors. Compute (by eq. (6) in ohmic),

$$V_T(V_{SB}) = V_{GS} + \frac{\beta V_{DS}^2 + I_{DS}}{\theta_{eff} I_{DS} - \beta V_{DS}} \quad (11)$$

(using for β and θ_{eff} the values extracted from Curve 1) and fit it to eq. (2) (using for V_{T0} the value extracted from Curve 1), obtaining $\{\gamma, \phi\}_{ohmic}$.

- 3) Measure Curve 3 for both transistors. Extract the *large signal parameters* $\{\beta, V_{T0}, \theta_{eff}\}_{sat}$.
- 4) Measure Curve 4 for both transistors. Compute (by eq. (6) in saturation),

$$V_T(V_{SB}) = V_{GS} - \frac{\theta_{eff} I_{DS}}{\beta} \left[1 + \sqrt{1 + \frac{2\beta}{\theta_{eff}^2 I_{DS}}} \right] \quad (12)$$

(using for β and θ_{eff} the values extracted from Curve 3) and fit it to eq. (2) (using for V_{T0} the value extracted from Curve 3), obtaining $\{\gamma, \phi\}_{sat}$.

At this point we have the *large signal parameters* for ohmic $\{\beta, V_{T0}, \theta_{eff}, \gamma, \phi\}_{ohmic}$ and saturation $\{\beta, V_{T0}, \theta_{eff}, \gamma, \phi\}_{sat}$. To obtain now the five *mismatch parameters* $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$ for the transistor pair, the procedure continues as follows,

- 5) For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 1 (see eq. (3))

$$\left. \frac{\Delta I_{DS}}{I_{DS}} \right|_1 = \frac{\Delta\beta}{\beta} + X_{1a} \Delta V_{T0} + X_{2a} \Delta\theta_o \quad (13)$$

compute the coefficients

$$X_{1a} = \frac{1 + \frac{1}{2} \theta_{eff} V_{DS}}{\left[V_{GS} - V_{T0} - \frac{1}{2} V_{DS} \right] [1 + \theta_{eff} (V_{GS} - V_{T0})]} \quad (14)$$

$$X_{2a} = \frac{V_{GS} - V_{T0}}{1 + \theta_{eff} (V_{GS} - V_{T0})}$$

using $\{V_{T0}, \theta_{eff}\}_{ohmic}$.

- 6) For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 2 (see eq. (3))

$$\left. \frac{\Delta I_{DS}}{I_{DS}} \right|_2 = \frac{\Delta\beta}{\beta} + X_{1b} \Delta V_{T0} + X_{2b} \Delta\theta_o + X_{3b} \Delta\gamma \quad (15)$$

compute the coefficients

$$X_{1b} = \frac{-\left(1 + \frac{1}{2} \theta_{eff} V_{DS}\right)}{\left[V_{GS0} - V_T - \frac{1}{2} V_{DS} \right] [1 + \theta_{eff} (V_{GS0} - V_T)]} \quad (16)$$

$$X_{2b} = \frac{V_{GS0} - V_T(V_{SB})}{1 + \theta_{eff} (V_{GS0} - V_T(V_{SB}))}$$

$$X_{3b} = X_{1b} [\sqrt{\phi + V_{SB}} - \sqrt{\phi}]$$

using $\{\theta_{eff}, \phi\}_{ohmic}$, where $V_{GS0} = 3.0V$ and $V_T(V_{SB})$ is obtained from eq. (11).

7) For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 3 (see eq. (3))

$$\left. \frac{\Delta I_{DS}}{I_{DS}} \right|_3 = \frac{\Delta\beta}{\beta} + X_{1c}\Delta V_{T0} + X_{2c}(\Delta\theta_o + \Delta\theta_e) \quad (17)$$

compute the coefficients

$$X_{1c} = -\frac{2 + \theta_{eff}(V_{GS} - V_{T0})}{(V_{GS} - V_{T0})[1 + \theta_{eff}(V_{GS} - V_{T0})]} \quad (18)$$

$$X_{2c} = -\frac{V_{GS} - V_{T0}}{1 + \theta_{eff}(V_{GS} - V_{T0})}$$

using $\{V_{T0}, \theta_{eff}\}_{sat}$.

8) For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 4 (see eq. (3))

$$\left. \frac{\Delta I_{DS}}{I_{DS}} \right|_4 = \frac{\Delta\beta}{\beta} + X_{1d}\Delta V_{T0} + X_{2d}(\Delta\theta_o + \Delta\theta_e) + X_{3d}\Delta\gamma \quad (19)$$

compute the coefficients

$$X_{1d} = \frac{2 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))}{(V_{GS0} - V_T)[1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))]} \quad (20)$$

$$X_{2d} = \frac{V_{GS0} - V_T(V_{SB})}{1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))}$$

$$X_{3d} = X_{1d}[\sqrt{\phi + V_{SB}} - \sqrt{\phi}]$$

using $\{\theta_{eff}, \phi\}_{sat}$, where $V_{GS0} = 3.0V$ and $V_T(V_{SB})$ is obtained from eq. (12).

9) Fit simultaneously eqs. (13), (15), (17) and (19) using the Least Squares Minimum (LSM) algorithm, obtaining the optimum five mismatch parameters $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$ for each transistor pair.

This measurement/extraction procedure is repeated for the 30 transistor pairs of equal size. For each extracted mismatch parameter ΔP ($\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma$) its standard deviation $\sigma_{(\Delta P)}$ is computed, as well as all correlations between pairs of mismatch parameters $r_{(\Delta P_1, \Delta P_2)}$. For each fabricated chip, standard deviations and correlations are obtained for each transistor size and type (NMOS and PMOS).

4. Mismatch Characterization Results

Statistical characterization of these five parameters results in five standard deviations $\sigma_\beta, \sigma_{V_{T0}}, \sigma_\gamma, \sigma_{\theta_o}, \sigma_{\theta_e}$ and 10 correlation coefficients for each transistor size, which can be used to predict the current mismatch standard deviation

$$\begin{aligned} \sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) &= \sigma_\beta^2 + \left(\frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_T}\right)^2 \left(\sigma_{V_{T0}}^2 + \left(\frac{\partial V_T}{\partial \gamma}\right)^2 \sigma_\gamma^2\right) + \\ &+ \left(\frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta}\right)^2 \left(\sigma_{\theta_o}^2 + \left(\frac{V_{DS_{eff}}}{V_{GS} - V_T}\right)^2 \sigma_{\theta_e}^2\right) + \text{correlation terms} \end{aligned} \quad (21)$$

Fig. 1 compares the measured values of $\sigma(\Delta I_{DS}/I_{DS})$ (shown with symbols) with those predicted by eq. (21) for the four measured curves of eqs. (10), for all 30 transistor sizes. As can be seen the agreement between measured and predicted mismatch is excellent. To our knowledge, such agreement has never been reported before using conventional mismatch models for such a wide range of transistor sizes, including short channel ($1\mu m$) transistors.

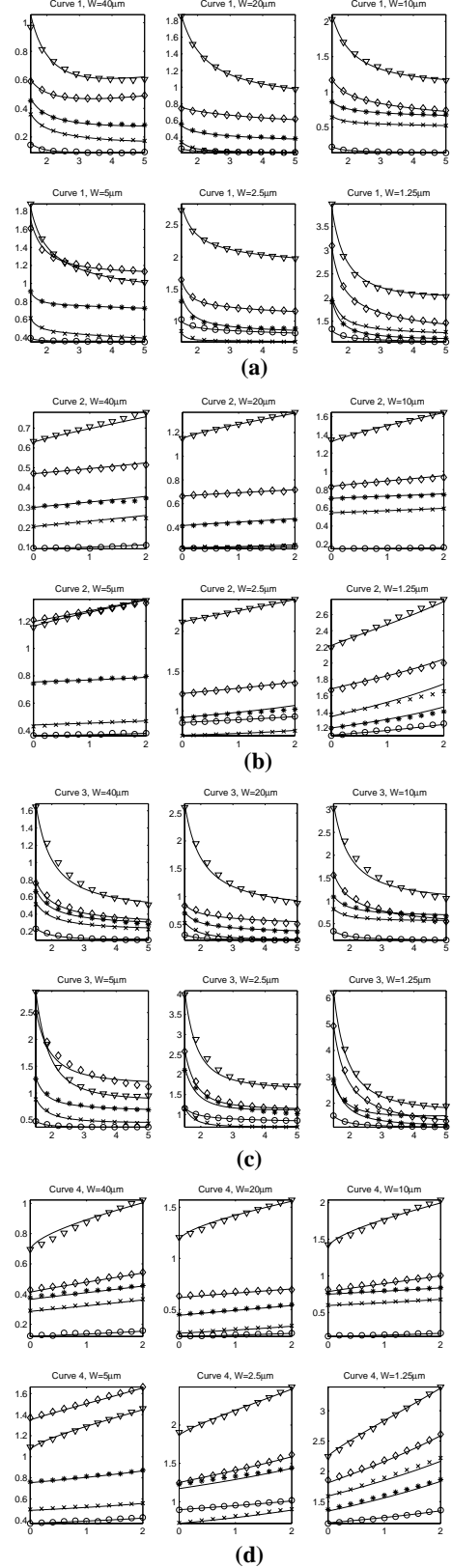


Fig. 1: Measured vs. Predicted Current Mismatch $\sigma(\Delta I_{DS}/I_{DS})$ (in %) for all transistor sizes for (a) Curve 1, (b) Curve 2, (c) Curve 3, (d) Curve 4. Symbols denote different transistor lengths: circles $L=40\mu m$, crosses $L=10\mu m$, stars $L=4\mu m$, diamonds $L=2\mu m$, triangles $L=1\mu m$.

Fig. 2 shows the values of the extracted standard deviations $\sigma(\Delta\beta/\beta)$, $\sigma(\Delta V_{T0})$, $\sigma(\Delta\gamma)$, $\sigma(\Delta\theta_o)$, $\sigma(\Delta\theta_e)$ as a function of transistor size. For each transistor size, 8 diamonds are shown, one for each of the 8 non-faulty measured chips. For simulation purposes, it is very convenient to have a dependence for the mismatch standard deviations as functions of transistors width W and length L . Many such dependencies have been proposed in the specialized literature [1], [2], [8]. In the present study we just intend to obtain a mathematical function able to fit the measured data. We do not intend to provide a physical interpretation to the resulting fitting coefficients. Consequently, we selected a very general mathematical function and let the fitting routines select the best coefficients for our data. The chosen mathematical function is

$$\sigma_{(\Delta P)}^2 = \sum_{m,n} \frac{C_{mn}}{(W - \epsilon_w)^m (L - \epsilon_l)^n} \quad (22)$$

where parameters C_{mn} , ϵ_w and ϵ_l are computed for each mismatch parameter ΔP . Using the 30×8 data points available for each standard deviation, the surfaces in Fig. 2 were obtained using standard least square fitting procedures. The resulting coefficients for eq. (22) are shown in Table 1 for each standard deviation for NMOS transistors.

Table 1: Resulting Fitted Parameters for Surfaces defined by eq. (22) for NMOS Transistors. Units for W, L are μm .

	C_{00}	C_{11}	C_{20}	C_{02}	C_{21}	C_{12}	C_{22}	ϵ_w	ϵ_l
$\sigma(\Delta\beta/\beta)$	4.7e-7	1.1e-3	2.1e-4	1.6e-4	-2.0e-3	2.2e-3	7.8e-4	0.14	-9.3e-1
$\sigma(\Delta V_{T0})$	3.5e-7	1.9e-4	1.1e-5	1.2e-6	2.5e-4	-1.8e-5	-1.8e-5	-1.1	7.9e-1
$\sigma(\Delta\theta_o)$	4.9e-8	-5.9e-6	-5.2e-7	2.4e-5	2.4e-4	-5.9e-4	4.7e-3	-5.7	-5.1e-2
$\sigma(\Delta\theta_e)$	5.5e-8	-4.8e-6	2.5e-6	1.0e-6	8.3e-5	3.1e-5	-7.0e-5	-2.1	8.3e-1
$\sigma(\Delta\gamma)$	1.5e-7	3.2e-5	1.7e-5	1.7e-6	2.0e-4	-2.4e-7	-5.4e-5	-1.1	5.5e-1

5. References

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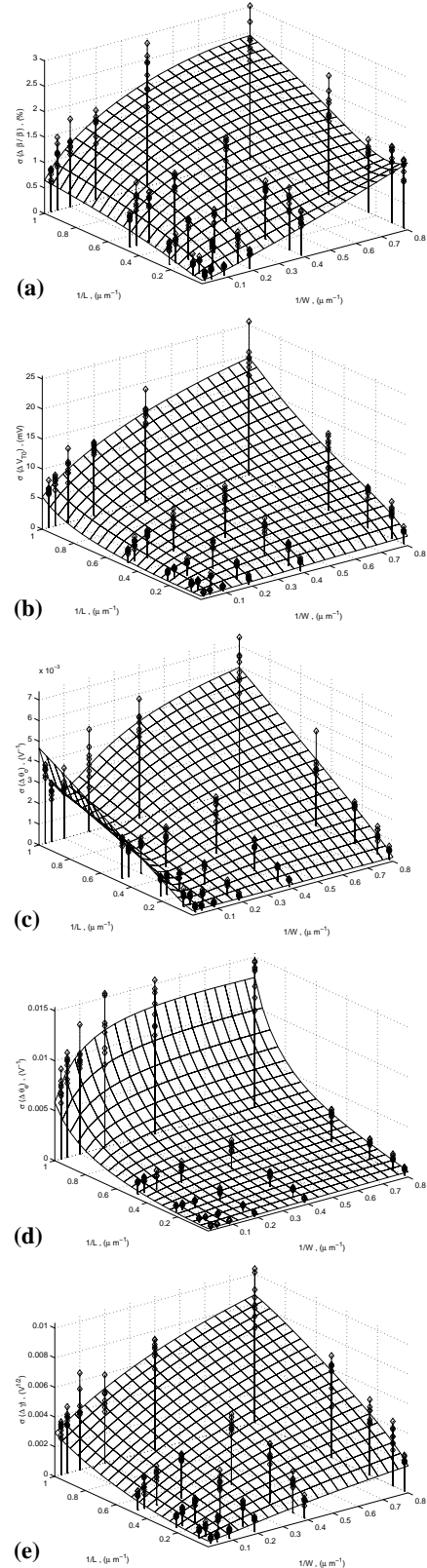


Fig. 2: Measured and fitted mismatch parameters for NMOS transistors. Diamonds are measured parameters for each transistor size and die. Surfaces correspond to fitted mathematical functions for (a) $\sigma(\Delta\beta/\beta)$, (b) $\sigma(\Delta V_{T0})$, (c) $\sigma(\Delta\theta_o)$, (d) $\sigma(\Delta\theta_e)$, (e) $\sigma(\Delta\gamma)$. Units for $1/W$ and $1/L$ axes are μm^{-1} .