On the Design and Characterization of Femtoampere Current-Mode Circuits

Bernabé Linares-Barranco and Teresa Serrano-Gotarredona

***Abstract*—In this paper, we show and validate a reliable circuit design technique based on source voltage shifting for current-mode signal processing down to femtoamperes. The technique involves specific-current extractors and logarithmic current splitters for obtaining on-chip subpicoampere currents. It also uses a special on-chip sawtooth oscillator to monitor and measure currents down to a few femtoamperes. This way, subpicoampere currents are characterized without driving them off chip and requiring expensive instrumentation with complicated low leakage setups. A special current mirror is also introduced for reliably replicating such low currents. As an example, a simple log-domain first-order low-pass filter is implemented that uses a 100-fF capacitor and a 3.5-fA bias current to achieve a cutoff frequency of 0.5 Hz. A technique for characterizing noise at these currents is also described and verified. Finally, transistor mismatch measurements are provided and discussed. Experimental measurements are shown throughout the paper, obtained from prototypes fabricated in the AMS 0.35-μm three-metal two-poly standard CMOS process.**

***Index Terms*—Analog VLSI design, leakage currents, mismatch, noise, subthreshold, ultralow currents, weak inversion.**

I. Introduction

HOW SMALL can we make the current in MOS transistors and still be able to build reliable circuits with them? The smallest MOS transistor current is limited by its leakage current. For example, in a typical present-day submicron CMOS process, the room temperature reverse diode leakage current of the drain or source diffusions of a minimum size transistor is typically around 10 aA (10^{-17}A). However, this current is usually not the one that limits the bottom current range of a MOS transistor. Because of ion implantation for lowering the threshold voltage of modern CMOS technologies, the effective leakage current (i.e., for $V_{\rm GS} = 0$) of minimum size MOS transistors may be as large as 10 pA. For example, Fig. 1(b) shows the simulated $I_{\rm DS}$ versus $V_{\rm GS}$ curves (with $V_{\rm DS} = V_{\rm DD}/2$, $V_{\rm DD} = 3.3$ V) of minimum size nMOS and pMOS transistors [as seen in Fig. 1(a)] for a 0.35-μm CMOS process, using the corner analysis parameters provided by the manufacturer. As can be seen, the worst case corner yields a minimum current of around 1 pA for a minimum size pMOS and more than 10 pA for a minimum size nMOS.

For $V_{\rm GS} = 0$ V (nMOS) or $V_{\rm GS} = V_{\rm DD}$ (pMOS), the MOS current has not reached the diode reverse current, yielding a much larger off current. Fig. 1(c) shows two experimentally measured $I_{\rm DS}$ versus $V_{\rm GS}$ curves. Curve $\rm nmos_{\it a}$ corresponds to a $W = 1$ μm/$L = 1$ μm nMOS transistor. The minimum cur-

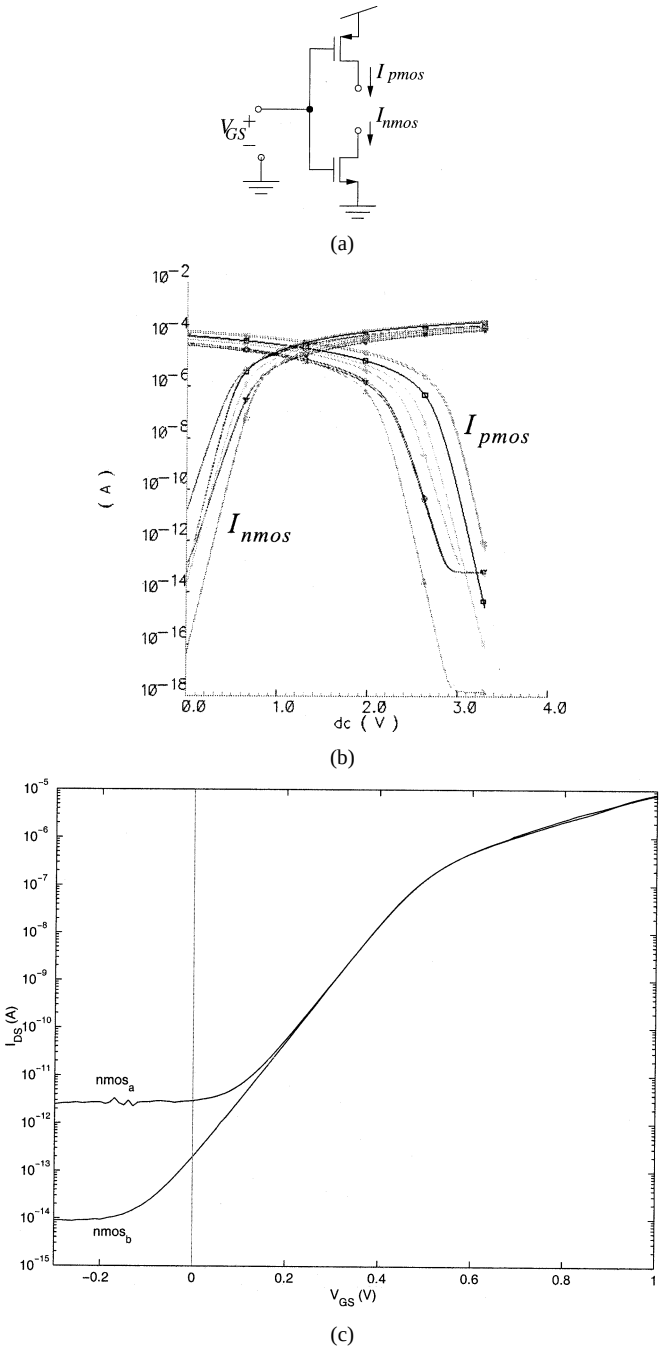

Fig. 1. Typical modern submicron CMOS nMOS and pMOS transistor $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics. (a) Schematic. (b) Corner analysis simulation. (c) Experimental measurements.

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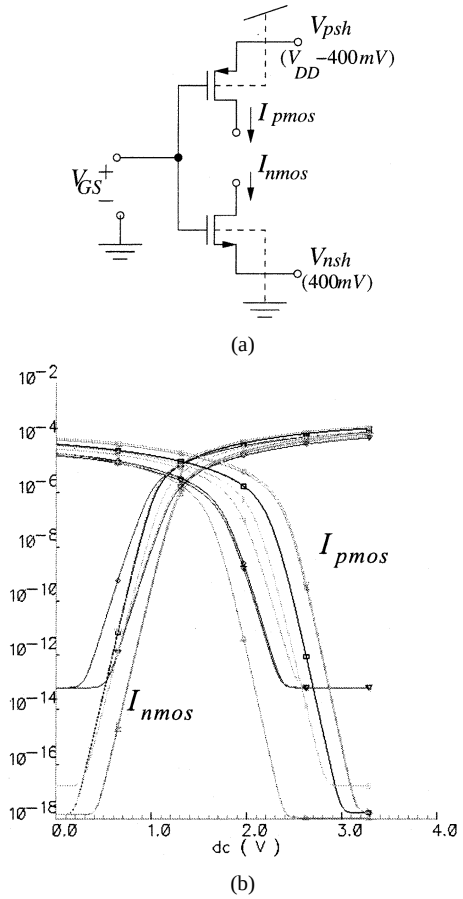


Fig. 2. Illustration of the source voltage shifting technique. (a) Circuit schematic. (b) Corner analysis simulated $I_{\rm DS}$ versus $V_{\rm GS}$ characteristics.

rent of several picoamperes is reached for $V_{\rm GS} \approx 100$ mV. This is the leakage current introduced by the pad protection diodes. Curve $\rm nmos_b$ corresponds to the parallel of 120 $\rm nmos_a$ transistors and dividing the measured current by 120. This way, the pad diodes current is divided by 120. As can be seen, there is transistor current well below $V_{\rm GS} = 0$ V.

In this paper, we will provide techniques for reliably exploiting MOS transistor operation down to a few femtoamperes, as well as measurement and characterization techniques for such small currents.

II. Source Voltage Shifting

The fundamental method for exploiting the complete available current range (down to the diffusion diodes reverse leakage currents) is by either biasing the gate voltages beyond the power supply rails [as done in Fig. 1(c)] or by slightly shifting the source voltages. For example, if for the transistors in Fig. 1 the source voltages are connected to around 400 mV with respect to the power supply rails [as shown in Fig. 2(a)], we recover the complete current range that the device physics allows us, as seen in the corner analysis simulation of Fig. 2(b). The corners with the highest leakage current (69 fA) are those obtained for high temperature (85 °C). However, if we can guarantee room temperature operation, the limiting current can be of the order of 10 aA (10^{-17} A) or less.[1] For the CMOS process used (AMS 0.35-μm) the reverse biased diffusion diodes' leakage current density is estimated by the foundry to be around 0.02 fA/μm^2 at room temperature. This current density has improved up to a factor of two to three with respect to previous CMOS processes over the last decade, which is not much. However, minimum diffusion sizes have been reduced significantly, from about 6 μm $\times$ 6 μm for a typical 2-μm process to about 1 μm $\times$ 1 μm for a 0.35-μm process. Consequently, minimum size transistor diffusion diode leakage has improved by about a factor of 100.

[1]In the simulations, the current resolution needs to be set accordingly for such low values. In our simulations, we set it to 10^{-18} A.

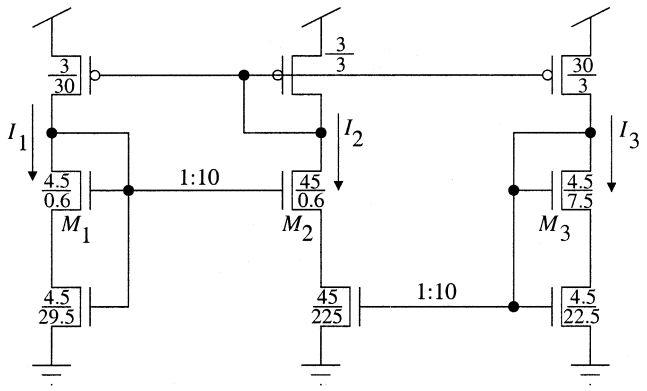


Fig. 3. Specific current extractor circuit.

Shifting the source voltage implies reducing the available voltage range. However, this is not a severe problem for subpicoampere current-mode circuits. Note that for such currents the gate-to-source voltage is extremely small (two or three hundreds of millivolts). Shifting the source voltage also implies the need for providing on-chip voltage sources V_{psh} and V_{nsh}. However, the shifted voltage values are not critical (as long as a minimum value is guaranteed) and the current driving capability of these on-chip sources is quite low. Consequently, from now on we will not consider the implementation of these sources.

The main drawbacks of operating at very low current levels are transistor noise and transistor mismatch, which are a consequence of operating the MOS transistors in the subthreshold regime [1]. Consequently, by operating at subpicoampere current levels, we inherit all the inconveniences of weak inversion. However, known weak inversion noise models seem to be preserved and relative current mismatch is supposed to stay constant within weak inversion operation. Experimental evidence of these facts will be shown in later sections.

III. On-Chip Inversion-Level-Based Current References

The process of threshold voltage adjustment in modern CMOS processes renders significant variations in the position of the weak inversion $I_{\rm DS}$ versus $V_{\rm GS}$ exponential curve [see Fig. 1(b) and Fig. 2(b)]. Consequently, biasing transistors deep inside the weak inversion region results in important variations in the required $V_{\rm GS}$ voltages. Furthermore, when working below picoamperes, a slight shift in $V_{\rm GS}$ voltage can turn the transistor off or produce decades of variation in the operating current. The position of the weak inversion $I_{\rm DS}$ versus $V_{\rm GS}$ exponential curve changes significantly not only from chip to chip (or wafer to wafer) but also with temperature [see Fig. 1(b) and Fig. 2(b)]. Fortunately, it suffers little variations for

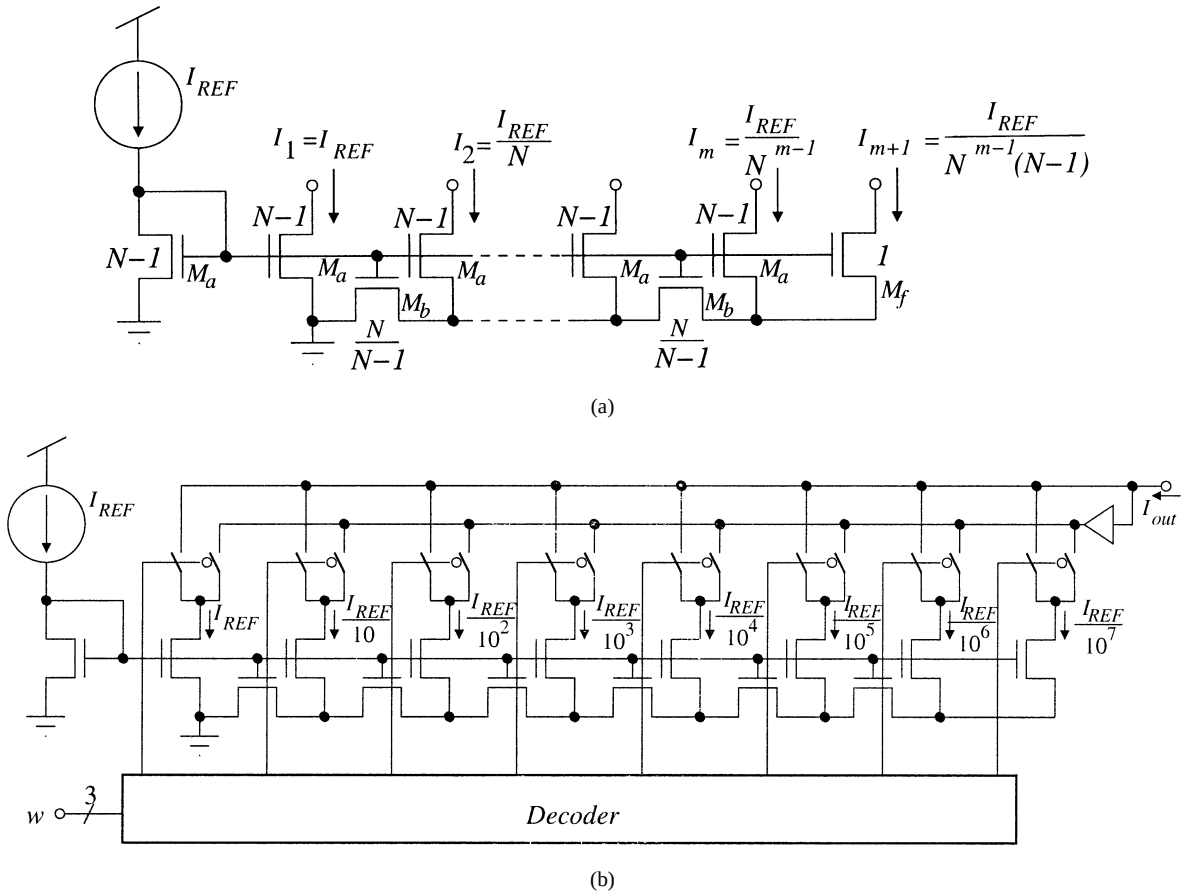


Fig. 4. (a) Circuit schematic for generic current splitting ratio N. (b) Implemented current splitter.

transistors within the same die (assuming constant temperature distribution). Consequently, the proper way to proceed is to design on-chip current references that are based on transistor inversion level [1], [3] and bias all transistors at predetermined inversion levels.

Present-day MOS models that provide continuous analytical functions for the transistor current from weak to strong inversion exploit the inversion level concept. The current is expressed as the difference between forward I_F and reversed I_R components

$$I_D = I_F - I_R = I_S(i_f - i_r)$$
$$I_S = 2\frac{W}{L}\mu C_{\text{ox}} n \phi_t^2 \tag{1}$$

where I_S is specific current, $\phi_t = KT/q$ is thermal voltage, n is subthreshold slope factor, and $i_f = I_F/I_S$, $i_r = I_R/I_S$ are the dimensionless inversion levels of the forward and reverse currents. Terminal voltages are related to the inversion levels by

$$V_P - V_S = \phi_t h(i_f)$$
$$V_P - V_D = \phi_t h(i_r) \tag{2}$$

where $V_P \approx (V_G - V_{T0})/n$ is the pinch-off voltage and $h(\cdot)$ is a nonlinear function. For the EKV model [1], it is a mathematical interpolation:

$$h(i) = 2\ln\left(\exp\left(\frac{1}{2}\sqrt{i}\right) - 1\right) \tag{3}$$

while for the ACM [3] model, it was derived from physical principles:

$$h(i) = \sqrt{1+4i} + \ln\left(\sqrt{1+4i} - 1\right) - 2 \tag{4}$$

The specific current I_S changes with process parameters and temperature, but if a circuit is designed so that transistors operate at predetermined inversion levels i_f and/or i_r then these will remain independent of process variations and temperature. To achieve this, an on-chip specific current I_S extractor circuit is required. Once I_S is available, transistors can be biased with scaled versions of it, thus assuring the desired inversion levels. For weak inversion operation, I_S needs not to be known with very high precision. Since there are several decades of available current range, I_S can usually be extracted with up to a factor of two error without significant impact. In our case, we used the circuit shown in Fig. 3 [4]. This circuit requires the I_3 branch to operate in strong inversion, the I_1 branch in weak inversion, and the I_2 branch in moderate inversion. For the sizes in Fig. 3, it autobiases M_3 at $i_{f3} = 4$. Since M_3 is in saturation, its reverse current can be neglected, resulting in

$$I_3 \approx 4I_{S3} = 4\frac{W_3}{L_3} I_{Sq} \tag{5}$$

where $I_{Sq} = 2\mu C_{\text{ox}} n \phi_t^2$ is transistor-size independent. In our case, we used a 0.35-μm CMOS process and designed I_3 to have a typical value of 1 μA, $I_2 = 100$ nA, and $I_1 = 10$ nA. Corner

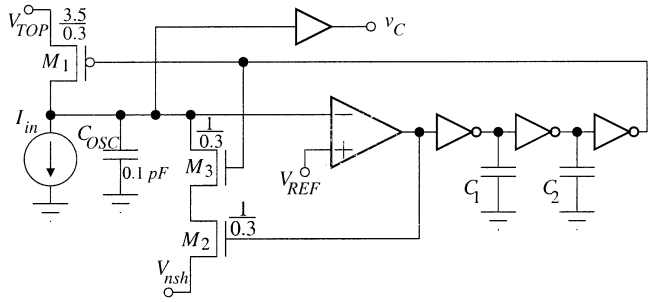


Fig. 5. Very low current-controlled sawtooth oscillator for on-chip subpicoampere current monitoring.

analysis simulations reveal that the maximum-to-minimum current ratio for these values is less than but close to 2.

IV. Current Splitting

The circuit in Fig. 3 is capable of providing a reference current in the order of nanoamperes. If we want to generate currents well below picoamperes, we can use the current splitting technique [5], [6]. The circuit in Fig. 4(a) illustrates this technique. The transistors have a size ratio of either $W/L = N-1$, $W/L = N/(N-1)$, or $W/L = 1$. This way, the current produced at the different output branches is progressively divided by a factor of N. In standard applications, this circuit is usually used with $N = 2$, thus providing a set of binary-weighted currents, which can be controlled digitally by means of switches to produce any combination of them. In our case, we are interested in obtaining very low currents. Consequently, in order to scale down $I_{\rm REF}$ quickly, we choose $N = 10$ and select only one of the output branches. The rest of the branches are connected to a voltage source providing a path for the currents, as shown in Fig. 4(b). The 3-bit digital word w selects one output branch to connect to node $I_{\rm out}$. Since w is a natural number between 0 and 7, the output current would be $I_{\rm out} = I_{\rm REF}/10^w$. According to Fig. 4(a), a splitter for $N = 10$ requires transistor M_f to be a unit transistor, M_a to be nine unit transistors, and M_b to be $9 \times 10 = 90$ unit transistors. To avoid too much leakage current because of such a high number of unit transistors, M_b was approximated to $W_b/L_b = 1$ (one unit transistor). Therefore, consecutive output currents will not have an exact ratio of 10, although close to 10, and we are still able to scale down $I_{\rm REF}$ quickly to a few femtoamperes.

V. On-Chip Low-Current Sawtooth Oscillator

Measuring femtoampere currents off chip is a cumbersome and tedious task which requires expensive instrumentation and very careful wiring and handling to avoid undesired parasitic leakage. To avoid all this, we designed a simple on-chip sawtooth oscillator driven by a current that sets its frequency of operation. The oscillator should keep operating for currents as small as the diffusion diodes' reverse currents. Using such an oscillator would allow us to have a reasonably good estimate of the currents we are injecting into it. The circuit is shown in Fig. 5. Input current $I_{\rm in}$ discharges capacitor $C_{\rm osc}$, while transistors M_1 and M_2 are OFF and M_3 is ON. Note that M_1 and M_2 have their source voltages shifted so that when their gates

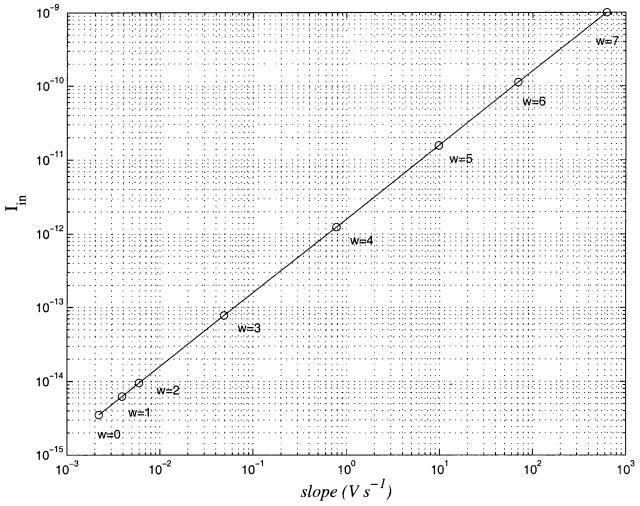


Fig. 6. Sawtooth oscillator inferred input currents versus measured slopes. $I_{\rm REF} = 1$ nA and digital control word w was set from 7 to 0.

are connected to $V_{\rm DD}$ and ground, respectively, they do not drive any current (only their reversed biased drain diffusion diode currents). As the capacitor voltage reaches $V_{\rm REF}$, the voltage comparator output will go from low to high. The positive feedback through transistor M_2 speeds this transition up significantly. After a small delay produced by the three inverters and capacitors C_1 and C_2, transistor M_3 is turned OFF while M_1 goes ON, recharging capacitor $C_{\rm osc}$ quickly to its starting value $V_{\rm TOP}$. This will make the comparator output trip back to low, which after the inverter chain delay turns M_1 again OFF and M_3 ON. At this point, input current $I_{\rm in}$ starts to discharge again $C_{\rm osc}$. The capacitor voltage v_C at $C_{\rm osc}$ is monitored through a high-speed analog buffer. This signal can be observed from outside the chip. The discharge slope at v_C is directly proportional to the discharge current $I_{\rm in}$

$$\text{slope} = \frac{\Delta v_C}{\Delta t} = -\frac{I_{\rm in}}{C_{\rm osc}}. \tag{6}$$

After measuring this slope with a known reference current (provided externally), we can infer the value of any in-chip current by comparing both slopes.

By combining the oscillator of Fig. 5 with the current splitter in Fig. 4(b), we can produce and measure extremely small currents. The reference current flowing into the current splitter was set externally to 1 nA. Extra switches are added so that the splitter output current can be driven off chip and measured precisely (calibrated). For the maximum current ($w = 7$), the splitter output was 1.05 nA. This value is used to derive $C_{\rm osc}$ in (6). Consequently, once $C_{\rm osc}$ is known (i.e., the oscillator is calibrated), any $I_{\rm in}$ in (6) can be inferred by measuring the corresponding discharging slope. Fig. 6 shows the inferred currents $I_{\rm in}$ versus the measured slopes for the eight possible values of the splitter control word w. The smallest inferred current was 3.51 fA, obtained when setting $w = 0$ and $I_{\rm REF} = 0$. This current value includes the sum of all leakage currents available at capacitor $C_{\rm osc}$ produced by the circuitry of the oscillator and the current splitter. Fig. 7 shows the oscillator inferred input currents when setting the digital control word w constant and equal to 3 while sweeping $I_{\rm REF}$ from 2 μA to 30 pA. Fig. 8

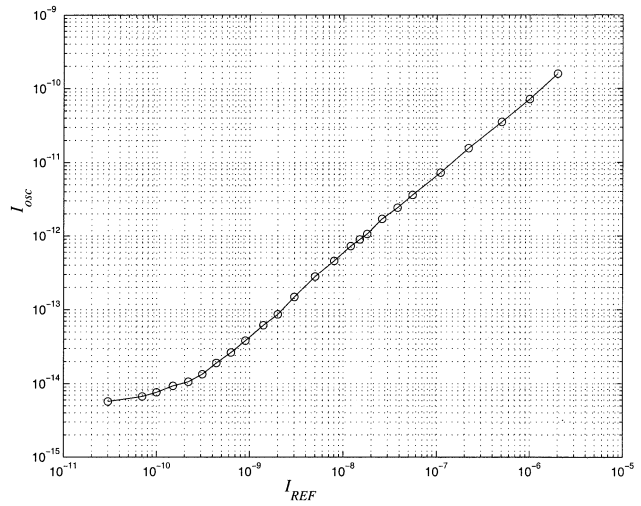


Fig. 7. Sawtooth oscillator inferred current versus $I_{\rm REF}$ while setting w constant equal to 3.

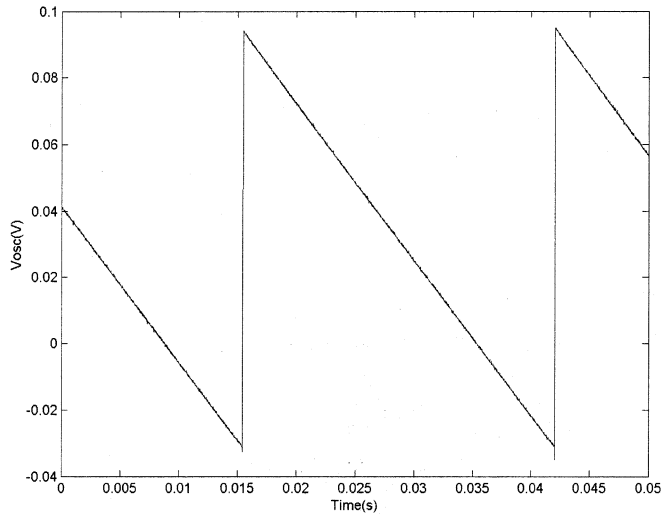


Fig. 8. Snapshots of oscillator for $I_{\rm REF} = 100$ nA while the control digital word w is maintained constant set to 3 ($I_{\rm osc} = 7$ pA).

shows one snapshot of waveform v_C for an oscillator input current $I_{\rm REF} = 100$ nA and the digital control word of the current splitter set to $w = 3$. The measured slope of the oscillator in this case is 4.7 V/s. According to Fig. 6, this slope corresponds to an oscillator input current of approximately 7 pA which also corresponds to the measurement shown in Fig. 7 for $I_{\rm REF} = 100$ nA.

VI. Subpicoampere Current Mirrors

A fundamental building block for any current-mode signal processing circuit is the current mirror. Fig. 9(a) shows the schematic of a conventional simple nMOS current mirror. Simulating its input–output characteristics by sweeping $I_{\rm in}$ from 10^{-17}A to 1 μA while performing corner analysis reveals the results shown in Fig. 9(b) (drain voltage of output transistor M_2 was connected to $V_{\rm DD}/2$). The worst case minimum operating current for this mirror is 15.6 pA, well above the worst case reverse biased diffusion diode currents. This is

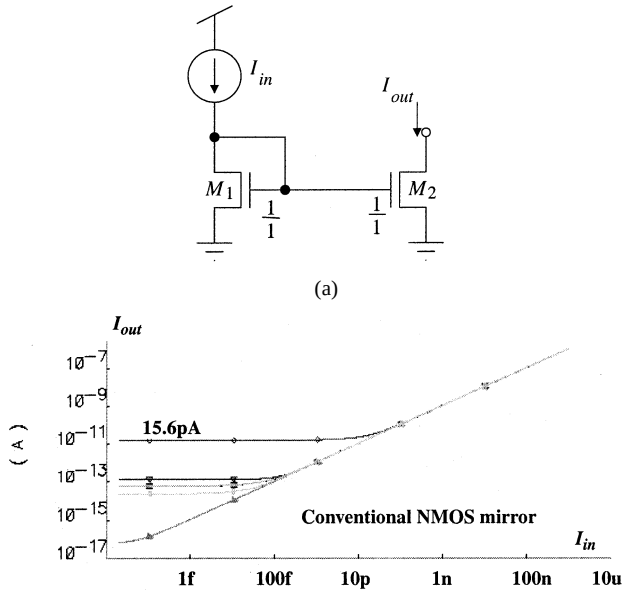


Fig. 9. Conventional simple current mirror. (a) Schematics. (b) Input–output current characteristics corner analysis.

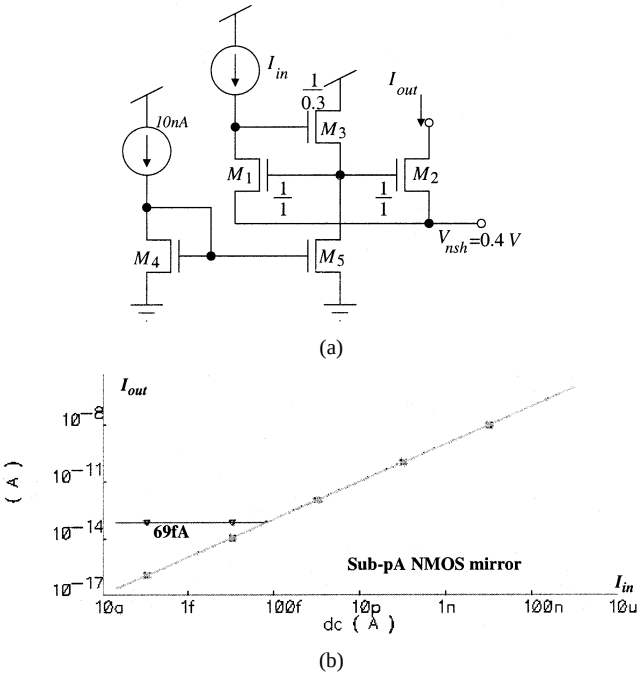


Fig. 10. New current mirror topology suitable for subpicoampere current operation. (a) Schematics. (b) Input–output characteristics corner analysis.

because transistors cannot be turned completely off. Shifting the source voltages for this mirror does not solve the problem because the gate voltage cannot go below the source voltage for this topology. Using the topology in Fig. 10(a) allows the gate voltage to adapt below the shifted source voltages. Transistors M_3–M_5 implement a voltage shifter that makes the gate voltage of M_1 one threshold voltage below its drain. Performing corner analysis simulations on this topology provides the results shown in Fig. 10(b). The high-temperature corners saturate at the diffusion diodes leakage currents (69 fA), while the others remain fully operative down to 10 aA (10^{-17}A).

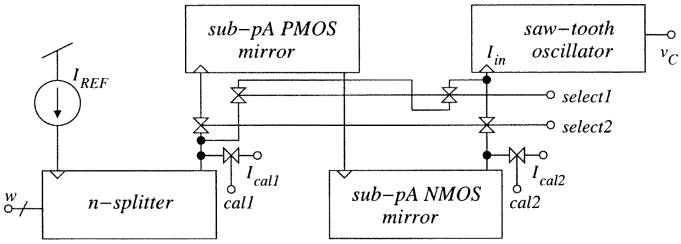


Fig. 11. Testing of subpicoampere current mirrors using current splitters and low current sawtooth oscillator.

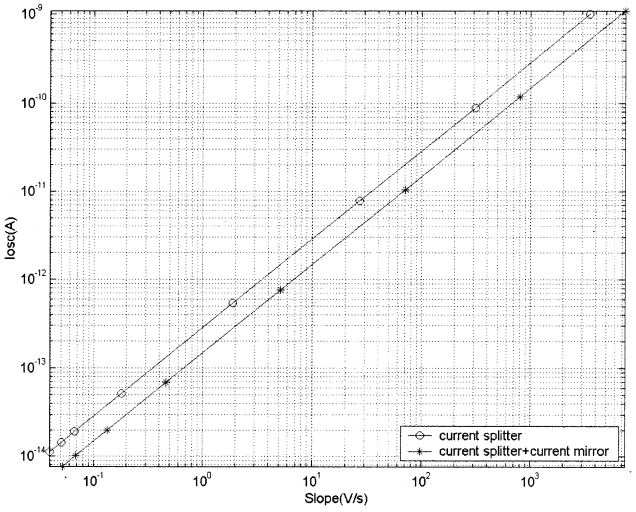
In order to experimentally test this current mirror topology, pMOS and nMOS versions were used in combination with the current splitter and the sawtooth oscillator, as shown in Fig. 11. By setting signal *select1* high (and all others low) the current splitter output is connected directly to the sawtooth oscillator. Setting *select2* high (and all others low) makes this current go through the two subpicoampere nMOS and pMOS current mirrors. By setting signal *cal1* high (and all others low), while setting the splitter to its maximum value, we can measure externally the maximum current provided by the splitter. This allows us to calibrate the slopes of the oscillator when it is connected directly to the splitter. By setting *cal2* high (and all others low), with the splitter at its maximum value, we calibrate the slopes for the case the two current mirrors are in the path. Note that $C_{\rm osc}$ in (6) is different if the mirrors are or are not in the path.

Fig. 12 shows the experimental results of this new subpicoampere current mirror topology. Fig. 12(a) shows the inferred input currents in the sawtooth oscillator versus the measured slope for the two above-mentioned situations: when the current splitter is directly connected to the input of the oscillator [curve marked with circles in Fig. 12(a)] and when the current goes through the combination of the nMOS and pMOS subpicoampere current mirrors [curve marked with stars in Fig. 12(a)]. From the results shown in Fig. 12(a), the curve in Fig. 12(b) can be inferred, which shows the current at the oscillator when the current splitter is connected directly to the oscillator [labelled Ics in Fig. 12(b)] versus the input current in the oscillator when the current from the current splitter goes through the combination of the nMOS and pMOS subpicoampere current mirrors [labelled Icm in Fig. 12(b)]. This way, the curve in Fig. 12(b) represents the input current (Ics)–output current (Icm) relation of the combination of the nMOS and pMOS subpicoampere current mirrors.

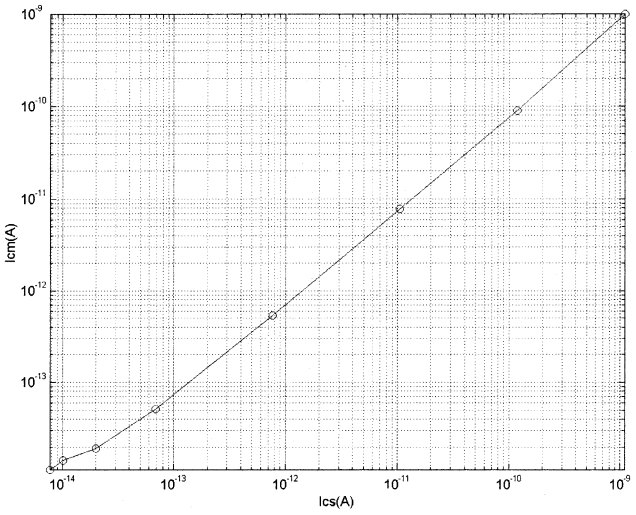
Another transistor topology appropriate for subpicoampere current processing, because it implicitly uses source voltage shifting, was reported elsewhere [7]. This topology adds the feature of clamping the mirror input voltage, at the expense of increasing circuit area and power consumption.

VII. Log-Domain Low-Pass Filter With Subhertz Cutoff Frequency

A very interesting application of subpicoampere current-mode signal processing is the capability of implementing extremely high time constant circuits. To illustrate this, a conventional first-order log-domain CMOS filter was fabricated and tested. The schematic of the selected first-order section



(a)



(b)

Fig. 12. Experimental results of the subpicoampere new current mirror topology. (a) Input current inferred in the sawtooth oscillator versus measured slopes when the current splitter is connected to the oscillator input and when the current goes through the nMOS and pMOS subpicoampere current mirrors. (b) Inferred input–output current behavior of the compound nMOS and pMOS subpicoampere current mirrors.

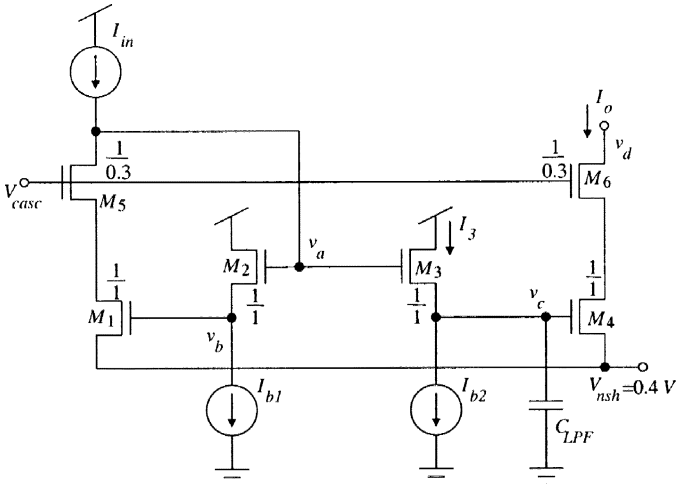


Fig. 13. Schematic of first-order log-domain low-pass filter section for subpicoampere operation.

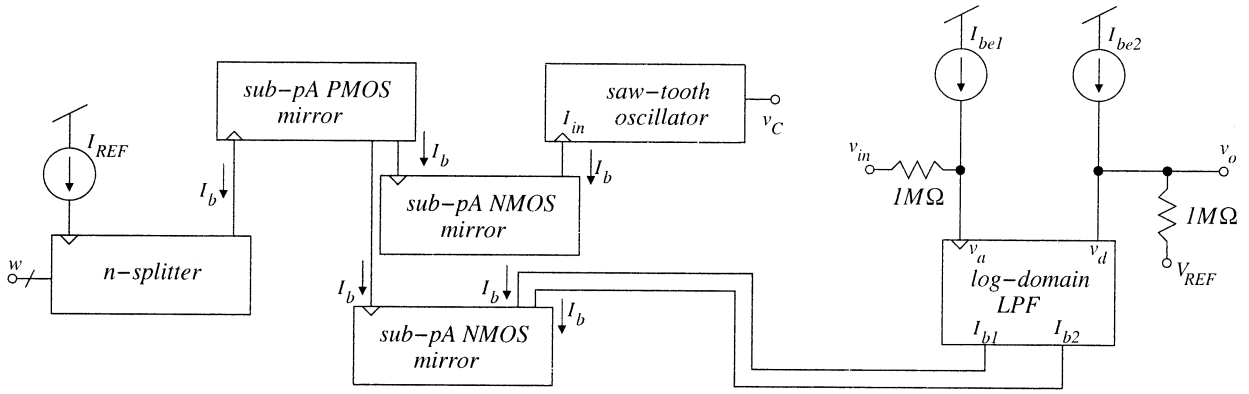


Fig. 14. Fabricated circuitry for test of subpicoampere log-domain low-pass filter.

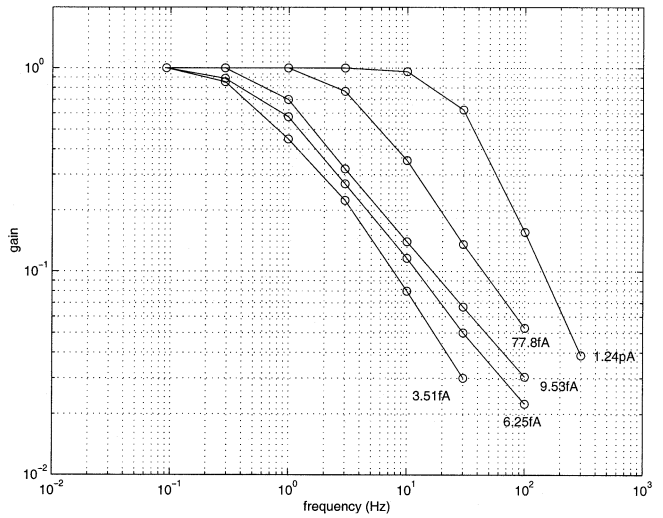


Fig. 15. Measured frequency response of the log-domain low-pass filter for different I_b values.

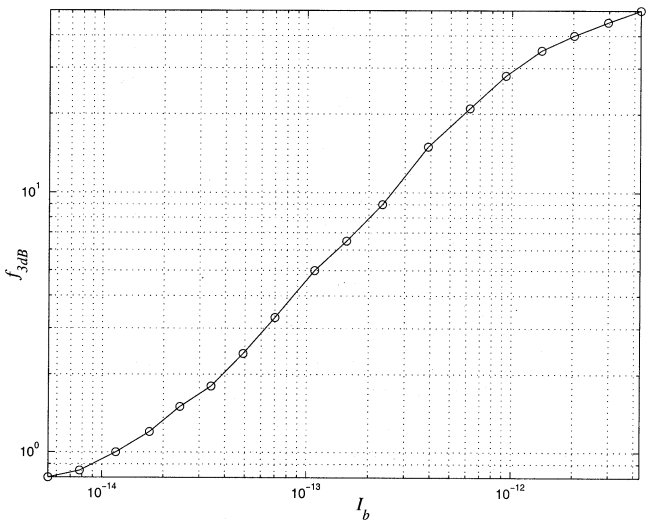


Fig. 16. Measured 3-dB cutoff frequency of low-pass filter when setting control word $w = 3$ and sweeping $I_{\rm REF}$ from 55 nA to 70 pA.

is shown in Fig. 13 [8]. M_5 and M_6 are cascode transistors for keeping the drain voltages of M_1 and M_4 equal. The low-pass filtering function is realized by transistors $M_1 - M_4$ and capacitor $C_{\rm LPF}$. Assuming all transistors in their weak inversion saturation region, the equations describing the circuit operation are

$$\begin{aligned} I_{\rm in} I_{b1} &= I_3 I_o \\ I_3 &= I_{b2} + C_{\rm LPF}\dot{v}_C \\ \dot{v}_C &= n\phi_t \frac{\dot{I}_o}{I_o}. \end{aligned} \tag{7}$$

Assuming $I_{b1} = I_{b2} = I_b$, (7) results in the following time domain differential equation:

$$\begin{aligned} I_{\rm in} &= I_o + \tau_{\rm LPF}\dot{I}_o \\ \tau_{\rm LPF} &= n\phi_t \frac{C_{\rm LPF}}{I_b} \end{aligned} \tag{8}$$

which describes a first order low-pass filter with 3-dB cutoff frequency $\omega_{\rm LPF} = 1/\tau_{\rm LPF}$. For a 1-Hz cutoff frequency with $C_{\rm LPF} = 0.1$ pF, $n = 1.37$, and $\phi_t = 26$ mV, the bias current should be $I_b = 2\pi n\phi_t C_{\rm LPF} f_{\rm LPF} = 22.4$ fA.

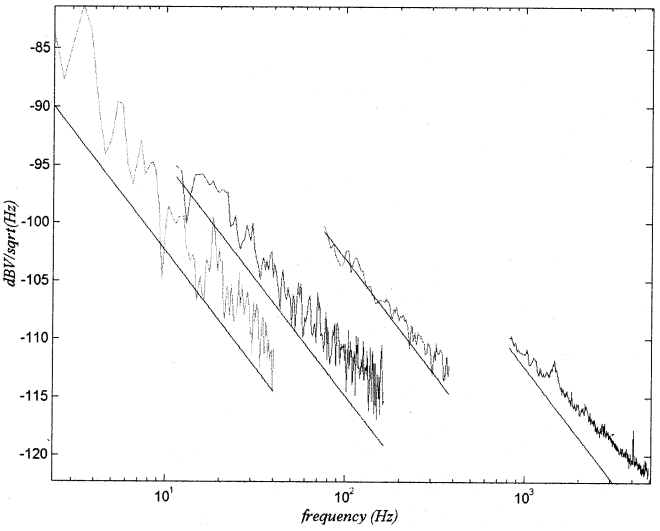


Fig. 17. Measured spectral noise density at discharging oscillator capacitor.

The log-domain low-pass filter of Fig. 13 with $C_{\rm LPF} = 0.1$ pF was fabricated in a 0.3-μm CMOS process together with an nMOS current splitter, a sawtooth oscillator, and a set of subpicoampere current mirrors, as shown in Fig. 14.

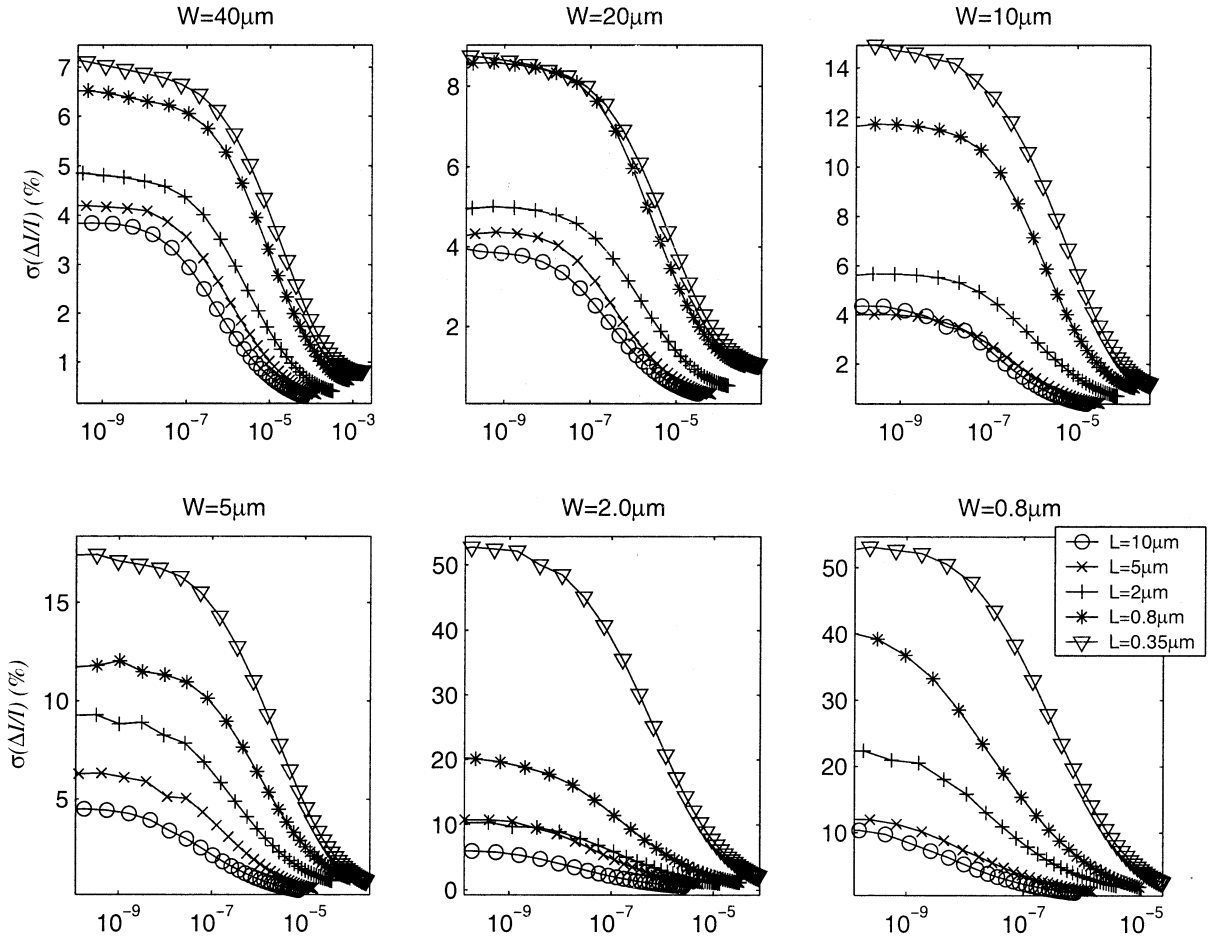


Fig. 18. Mismatch measurements for transistors of 30 different sizes in a 0.35-μm CMOS process. Vertical scale shows relative current mismatch standard deviation in percent. Horizontal scale shows bias current.

Current $I_{\rm REF}$ for the current splitter was supplied off chip, as well as I_{be1}, I_{be2}, and the two 1-MΩ resistors. I_{be1}, I_{be2}, and $V_{\rm REF}$ were adjusted to make the dc values $v_a = v_d$ and the low-pass transfer function was measured from $v_{\rm in}$ to v_o. The setup in Fig. 14 allows us to control the value of $I_{b1} = I_{b2} = I_b$ of the low-pass filter, while inferring that value by means of the sawtooth oscillator. Fig. 15 shows the measured low-pass filter frequency response for several values of I_b. Here $I_{\rm REF}$ was set to 1 nA and the digital control word w changed from 1 to 5. The values of the 3-dB cutoff frequency were, respectively, 0.5, 0.7, 1.0, 3.5, and 25 Hz, while I_b was inferred to be 3.51 fA, 6.25 fA, 9.53 fA, 77.8 fA, and 1.24 pA (using the sawtooth oscillator method of Section V). When keeping $w = 3$ constant and changing $I_{\rm REF}$ from 55 nA down to 70 pA, the set of values $f_{\rm 3dB}$ versus I_b of Fig. 16 were measured. Figs. 15 and 16 were not measured using a spectrum/network analyzer, because the frequencies were too low. Instead, input and output sinusoids were directly observed on an oscilloscope and the output waveform amplitude was manually measured as a function of input frequency.

VIII. Noise Estimation

It is possible to estimate the noise produced by the subpicoampere MOS transistors by simply observing the sawtooth oscillator waveforms. Measuring its frequency jitter is not a good way because it is produced not only by the input current noise but also by the comparator input equivalent noise. However, if we look at the sawtooth oscillator wave only during the time intervals that capacitor $C_{\rm osc}$ is being discharged, the voltage noise observed at the capacitor is produced by the input current noise and the analog buffer noise (see Fig. 8). Designing this buffer with sufficiently low noise, the noise observed at its output will be produced by the very low currents discharging capacitor $C_{\rm osc}$. Naturally, the voltage noise observed at the output will be an integrated version of the input current noise. Consequently, if the input current noise is white thermal noise, we should observe a $1/f^2$ (-20 dB/dec) output voltage noise.

To measure the noise we proceeded as follows. The oscillator waveforms were recorded using a 16-bit analog-to-digital converter for several values of the input current. The discharging slopes were isolated and fitted to straight lines. These lines were subtracted from the discharging slopes resulting in zero mean noise signals. These signals were analyzed using Welch's method for spectral estimation [10]. The results are shown in Fig. 17 for capacitor discharge currents equal to 7 fA, 40 fA, 600 fA, and 7 pA. Naturally, the noise spectral density could only be measured to frequencies as low as the sawtooth frequency itself. Even more, for frequencies close to the oscillation frequency, spectral content estimation can be mistaken by

distortion in the discharging slope. As can be seen in Fig. 17, all four noise measurements show the expected -20 dB/dec slope. Consequently, only white noise is being produced by the input currents for the observed frequency ranges. The thermal (white) noise power spectral density expected to be produced by weak inversion MOS transistors is [9]

$$\sigma_I^2 = 2qI \tag{9}$$

where q is the electron charge. Since this current noise is integrated on capacitor $C_{\rm osc}$ during the discharging ramps, the voltage noise present at its terminal will be

$$\sigma_V = \frac{\sigma_I}{2\pi f C_{\rm osc}}. \tag{10}$$

This theoretical noise is also shown in Fig. 17, for each discharging current, with straight lines. As can be seen, the measured noise resembles reasonably closely the theoretically predicted noise.

Flicker noise should become noticeable by lowering the operating frequencies. However, note that with this noise measurement method the lowest measurable frequency is limited by the sawtooth signal frequency, which is directly proportional to the biasing current. The total equivalent gate voltage spectral noise density for a subthreshold MOS is given by [2]

$$\sigma_{V_G} = \sigma_{\rm flicker} + \sigma_{\rm thermal} = \frac{4KT\rho}{WLf} + \frac{2qI}{g_m}. \tag{11}$$

We can calculate the relation between bias current and frequency for which thermal and flicker noise in subthreshold are equal:

$$\frac{f_c}{I} = \frac{4\rho}{n^2\phi_t WL}. \tag{12}$$

For our process, $\rho = 0.5$ Vm^2/As, which means that for a 1μm $\times$ 1μm transistor, flicker and thermal noise densities become equal when

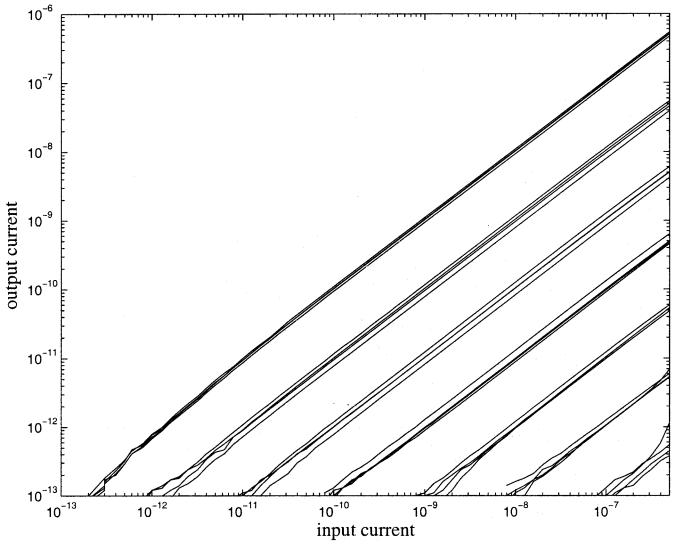
$$\frac{f_c}{I} = 4 \times 10^{-13} A^{-1} s^{-1}. \tag{13}$$

Consequently, for $I = 7$ pA, $f_c = 280$ Hz, for $I = 600$ fA, $f_c = 24$ Hz, for $I = 40$ fA, $f_c = 1.6$ Hz, and for $I = 7$ fA, $f_c = 2.8$ Hz. Note that all these frequencies fall outside the measured ranges in Fig. 17, limited by the sawtooth waveform frequencies.

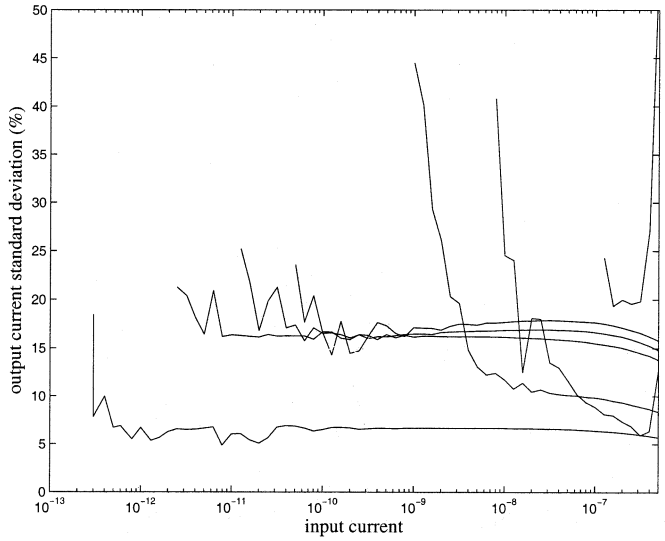
IX. Mismatch Considerations

Mismatch is a nonideal effect that becomes stronger for weak inversion operation. However, present-day MOS transistor models predict that relative current mismatch should tend to stay constant when entering this bias regime [2]. We have performed mismatch measurements on devices of 30 different sizes in a 0.35-μm CMOS process, for currents ranging from strong to weak inversion. The currents were measured using an external instrument, thus limiting the minimum measurable current. Furthermore, they were measured using a mismatch measurement chip [11] where 1920 transistors (30 sizes $\times$ 8 rows $\times$ 8 columns) are connected in parallel and only one does not have its gate shorted to its source. This implies that 1920 drain diffusions are in parallel, contributing a significant leakage current. The results can be seen in Fig. 18, where the minimum current for which mismatch could be measured was around 100 pA. However, we can see the tendency of mismatch becoming constant as the transistors are biased deeper inside weak inversion. This is predicted by the theory of modern single-equation MOS models that are continuous from strong to weak inversion [2], [3]. We might expect that, as we decrease the operating current below the picoamperes, the relative current mismatch should keep constant.

As an illustrative example, we measured the four fabricated samples of the current splitter in Fig. 4, using an off-chip



(a)



(b)

Fig. 19. Mismatch measurements for the current splitter in Fig. 4. (a) Measured input–output currents for the top seven splitter outputs and the four fabricated samples. (b) Computed relative standard deviation for the currents in (a).

instrument, and sweeping the input current from 100 fA to 0.5 μA. The resolution of the instrument was limited to about 100 fA. We measured the splitter output currents at seven of the eight possible outputs (the eighth output gave only leakage). Although we measured only four samples, we were able to estimate the order of magnitude of the mismatch between transistors inside each chip. Fig. 19(a) shows the measured output current versus the input reference current for the seven top output branches of the splitter. The measured data for the four fabricated samples are superimposed. Fig. 19(b) is the result of computing the relative standard deviation for the curves in Fig. 19(a), expressed in percentages. As we can see, the relative mismatch tends to stay below 20% and at current independent values. For subpicoampere operation, we expect to observe the same behavior, as predicted by the theory [2].

X. Conclusion

We have shown that it is possible to design and reliably exploit femtoampere current-mode circuits. The fundamental method is to use source voltage shifting. Currents in the range of picoamperes and well below can be reliably generated on-chip by means of inversion-level-based specific-current extractors and logarithmic current splitters. To monitor subpicoampere currents, a simple current-driven sawtooth oscillator can be included on chip. An appropriate subpicoampere current mirror topology has been introduced as well, for proper current replication at such low values. As an application, a very simple low-pass filter was designed, fabricated, and tested. It was based on log-domain circuit techniques. It uses six small-size transistors and a 100-fF capacitor and provides a 3-dB cutoff frequency of 0.5 Hz when biased with 3.51 fA. It is shown how noise measurements can be easily performed on transistors operating down to femtoamperes, and how such measurements resemble closely enough the corresponding theoretical predictions. Mismatch measurements are included, although for higher currents. Temperature measurements are reported elsewhere [12].

In conclusion, we have shown that it is possible to exploit subpicoampere operation for modern standard CMOS technologies. Important drawbacks, however, are noise and mismatch. From the previous discussions on noise and mismatch, one concludes that by lowering the operating currents, both noise and mismatch effects will stay constant and independent of current level for the complete weak inversion regime (either above or below subpicoampere operation). From Fig. 18, we may expect that further current reductions will not degrade mismatch, as predicted by the theory. However, this has not been verified experimentally. From (11), we can see that the equivalent gate-voltage noise of a MOS transistor is also current independent, because the ratio I/g_m is constant for weak inversion [2], [3]. Since the noise model used in (11) is the same as used in Fig. 17 to compare theory and measurements for current as low as 7 fA, we have solid reasons to believe that this noise model is still valid for such low currents. Consequently, it seems that the noise and mismatch behavior of MOS transistors is not degraded as operating current is lowered well below picoamperes, and that MOS transistors can be used as in traditional weak inversion designs (biased around nanoamperes). However, it is also true that to obtain such low currents one needs to minimize the area of drain (and possibly also source) diffusions. This implies using small transistor widths, which will limit both mismatch and noise. Therefore, there will be a noise and mismatch limitation which will reduce the possible applications for circuits exploiting these low currents. Mismatch could be compensated through calibration techniques [13].

Interesting applications where such low current circuits can be used are those that require very low time constants. Since mismatch is important, the precision in the time constant value will be low (unless calibration is used). Also, the applications should be tolerant to high noise. Another field where very low currents need to be handled is in low light photo sensors, where operating currents become close to dark currents (fractions of femtoamperes). In general, ultralow-current techniques are beneficial in circuits where leakages are critical, as in dynamic memories.

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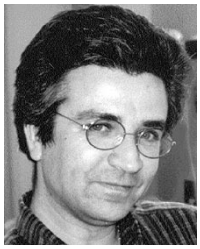

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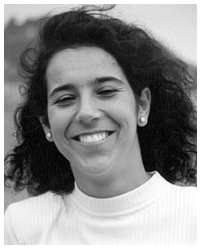

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