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Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation

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Abstract. This paper presents a methodology for characterizing the random component of transistor mismatch in CMOS technologies. The methodology is based on the design of a special purpose chip which allows automatic characterization of arrays of NMOS and PMOS transistors of different sizes. Up to 30 different transistor sizes were implemented in the same chip, with varying transistors width W and length L. A simple strong inversion large signal transistor model is considered, and a new five parameters MOS mismatch model is introduced. The current mismatch between two identical transistors is characterized by the mismatch in their respective current gain factors $\Delta\beta/\beta$, threshold voltages ΔV_{T0}, bulk threshold parameters $\Delta\gamma$, and two components for the mobility degradation parameter mismatch $\Delta\theta_o$ and $\Delta\theta_e$. These two components modulate the mismatch contribution differently, depending on whether the transistors are biased in ohmic or in saturation region. Using this five parameter mismatch model, an extraordinary fit between experimental and computed mismatch is obtained, including minimum length (1 μm) transistors for both ohmic and saturation regions. Standard deviations for these five parameters are obtained as well as their respective correlation coefficients, and are fitted to two dimensional surfaces $f(W, L)$ so that their values can be predicted as a function of transistor sizes. These functions are used in an electrical circuit simulator (Hspice) to predict transistor mismatch. Measured and simulated data are in excellent agreement.

Key Words: analog integrated circuits, transistor mismatch, transistor model, transistor parameter extraction, circuit simulation

1. Introduction

Precise analog CMOS circuit design requires availability of confident transistor mismatch models during the design and simulation stages. During the design phase of an analog VLSI circuit, designers face many constraints imposed by the design specifications, such as speed, bandwidth, noise, precision, power consumption, area consumption, which need to be traded off for optimum overall performance. Designers must rely on accurate simulation tools in order to achieve a well optimized final design, especially if performance is pushed to the limits allowed by a given technology. Simulation tools are reliable as long as they are based on good models obtained through confident characterization techniques. If good and well characterized models are embedded in a reliable simulator, circuit designers can confidently test different circuit topologies and optimize each one of them by optimally sizing their transistors. Automatic design tools are available that by interacting with a simulator are able to obtain transistor sizes for close-to-optimum performance for a given circuit topology and a set of design constraints [1–5].

Often it is not possible to simulate properly the precision limits that can be achieved by a certain circuit topology in a given fabrication process because VLSI circuit manufacturers rarely provide transistor mismatch information, and, if they do, its dependence on transistor size (width and length, independently[1]) is not known. What is common among VLSI manufacturers is to provide ''*Slow*'', ''*Typical*'' and ''*Fast*'' transistor models which account for the range of variation in transistor electrical parameters from run to run (or wafer to wafer, or die to die). Consequently, for a fabricated die, all transistors will

have the same model, which should lie somewhere in between the ''*Slow*'' and ''*Fast*'' models. However, this does not account for the variation in transistor electrical parameters whithin the same die. Such variation is often referred in the specialized literature as ''*transistor mismatch*''. Transistor mismatch affects offset voltage of differential pairs, errors in current mirrors, errors in arrays of identical current sources, ... It is the information on the behavior of this transistor mismatch which is rarely provided by VLSI manufacturers and, if they do, the information is very limited. In this paper we provide a very simple and cheap methodology circuit designers can use to characterize transistor mismatch as a function of transistor width and length, and how to use this information to predict mismatch effects in circuit simulators.

In the specialized literature transistor mismatch is usually characterized by providing the standard deviation of the mismatch in a set of transistor electrical parameters such as the threshold voltage V_{T0}, the current gain factor $\beta = \mu C_{ox} W/L$ (μ is mobility, C_{ox} is gate oxide capacitance density, W is transistor width, and L is transistor length), the mobility degradation parameter θ, and the bulk threshold parameter γ. Table 1 shows a few examples [6–11] on what dependencies for $\sigma^2_{(\Delta\beta/\beta)}$, $\sigma^2_{(\Delta V_{T0})}$, $\sigma^2_{(\Delta\theta)}$ and $\sigma^2_{(\Delta\gamma)}$ on transistor sizes (W is transistor width, L is transistor length) and distance D have been postulated. A good study [12] based on BSIM transistor models is also available in the literature.

In the present paper we introduce a new mismatch model in which the mismatch in θ is separated into two components, characterized by $\Delta\theta_o$ and $\Delta\theta_e$, which modulate their contribution differently depending on whether the transistor is biased in ohmic or saturation region. As we will see later, this provides excellent agreement between measured and predicted mismatch for ohmic and saturation regions, even for minimum length transistors. In the next Sections we introduce an experimental method to obtain a relatively high number (30) of samples (of $\sigma^2_{(\Delta\beta/\beta)}$, $\sigma^2_{(\Delta V_{T0})}$, $\sigma^2_{(\Delta\theta_o)}$, $\sigma^2_{(\Delta\theta_e)}$, $\sigma^2_{(\Delta\gamma)}$ and their correlations) in the $\{W, L\}$ design space. Then we fit these measured samples to a general nonlinear function of the form

$$\begin{aligned}\sigma^2_{(\Delta P)} &= C_{00} + \frac{C_{10}}{W-\varepsilon_w} + \frac{C_{01}}{L-\varepsilon_l} \\ &\quad + \frac{C_{20}}{(W-\varepsilon_w)^2} + \frac{C_{11}}{(W-\varepsilon_w)(L-\varepsilon_l)} \\ &\quad + \frac{C_{02}}{(L-\varepsilon_l)^2} + \cdots \\ &= \sum_{n,m} \frac{C_{nm}}{(W-\varepsilon_w)^n (L-\varepsilon_l)^m} \end{aligned} \quad (1)$$

where ΔP is the observed mismatch in a certain electrical parameter. Note that we are not interested in discovering the physical meaning of coefficients C_{nm}, ε_w, ε_l, but only in obtaining a good approximation for the function $\sigma^2_{(\Delta P)} = f(W, L)$ in order to use it confidently in a circuit simulator. By defining the space $\{x = 1/W, y = 1/L\}$, note that the limits in this space available to the circuit designer are $x_{\max} = 1/W_{\min}$, $y_{\max} = 1/L_{\min}$, $x_{\min} = 0$, $y_{\min} = 0$. Measuring a reasonable high number of sample points in this $\{x, y\}$ space provides sufficient information to interpolate the functions $\sigma_{(\Delta P)}$, which are fairly smooth in this space.

The paper is organized as follows. The next Section describes the mismatch characterization chip used to obtain all characterization data. Section 3 explains the set of curves measured for each transistor, how mismatch parameters were extracted from these curves, and how these parameters were statistically characterized. Section 4 provides characterization results for a digital $1.0\,\mu$m CMOS technology for a wide range of transistor sizes, and explains how these data were fitted to express standard deviations and correlations as a function of transistor sizes. Section 5 is intended to test the

Table 1. Examples of mismatch models in the literature.

	$\sigma^2_{(\Delta\beta/\beta)}$	$\sigma^2_{(\Delta V_{T0})}$	$\sigma^2_{(\Delta\theta)}$	$\sigma^2_{(\Delta\gamma)}$
Pelgrom [6]	$\frac{A_s^2}{WL} + \frac{A_w^2}{W^2L} + \frac{A_L^2}{WL^2} + S_\beta^2 D^2$	$\frac{A_{V_{T0}}^2}{WL} + S_{V_{T0}}^2 D^2$	—	$\frac{A_\gamma^2}{WL} + S_\gamma^2 D^2$
Laksh. [7]	$\frac{A_{\beta 1}}{WL} + \frac{A_{\beta 2}}{W^2+L^2}$	$\frac{A_{V0}}{WL}$	—	—
Bastos [9–11]	$\frac{A_\beta^2}{WL}$	$\frac{A_{V1}^2}{WL} + \frac{A_{V2}^2}{WL^2} - \frac{A_{V3}^2}{W^2L}$	$\frac{A_\theta^2}{WL}$	—

correctness and robustness of the extracted mismatch parameters, and finally Section 6 describes how to use the extracted mismatch characterization results in a standard circuit simulator like (H)Spice.

2. Mismatch Characterization Chip

According to Table 1 [6–11], the mismatch in parameter P between two identical transistors is statistically characterized by a quadratic deviation whose general form can be written as

$$\sigma^2_{(\Delta P)} = f(W, L) + S_P^2 D^2 \quad (2)$$

where W and L are the transistors width and length, and D is the distance between them. The presence of two terms in equation (2) indicates that there are two kinds of causes producing transistor mismatch. The first term is produced by the fact that **device physical parameters** (such as doping concentrations, junctions depth, implants depth, oxide thicknesses,...) are not exactly constant but suffer from random perturbations along a die. By increasing transistor areas the **device electrical parameters** P (like threshold voltage V_{T0}, current gain factor β, mobility reduction parameter θ, or bulk threshold parameter γ) will become less sensitive to the random nature of the **device physical parameters**. The second term in equation (2), characterized by parameter S_P, is produced by the fact that the **device physical parameters** present a certain gradient variation along the dies [6,8,10–13]. Usually, the gradients present in small and medium size dies can be approximated by planes. Statistical characterization of these planes (which means obtaining S_P) can be performed with a small number of transistors per die and measuring many dies. This is illustrated in Fig. 1 where three planes of different orientation are shown. Each plane represents the gradient variation of a given electrical parameter P for three different dies. If two transistors are located at positions (x_1, y_1) and (x_2, y_2) their gradient-induced mismatch contribution to ΔP is different for each of the three fabricated chips. However, for a given fabricated chip, the gradient plane is common for all transistors and the mismatch it induces can be eliminated through layout techniques, such as ''*common centroid*'' configurations [14]. Note that increasing transistor distance results in increasing the gradient-induced mismatch. Many Silicon Foundries do characterize, at the wafer level, these gradient variations, which stay fairly stable from wafer to wafer, and run to run. However, fabricated dies proceed from many wafer regions and therefore, their gradient component can be considered to possess a random nature. Characterization of the gradient random nature, which requires the availability of many dies, results in obtaining term S_P. On the other hand, the transistor mismatch induced by the **device physical parameters** random nature, changes little from die to die. Consequently, its statistical characterization can be done by putting many transistors in a single die and measuring a reduced number of dies. For example, for one of the dies in Fig. 1, by measuring ΔP of many transistor pairs separated by the same distance (and oriented in the same direction) and computing their standard deviation $\sigma_{(\Delta P)}$, the gradient induced component (characterized by $\overline{\Delta P}$) is eliminated, remaining only the random-induced component. This is very convenient for circuit designers, since they can easily have a small number of samples of a prototype mismatch-characterization-chip at a reasonable cost. This paper thus concentrates on the characterization of size dependent mismatch terms (i.e. $f(W, L)$ in equation (2)), and a wide range of transistor sizes will be characterized.

With all this in mind we designed a special purpose chip [15] intended to characterize the ''random perturbations induced terms'' of CMOS transistor mismatches, as a function of transistor size, i.e. function $f(W, L)$ in equation (2). As shown in Fig. 2, the chip consists of an array of identical cells. Each cell contains 30 NMOS and 30 PMOS transistors, each of a different size. Sizes are such that widths are $W = 40\,\mu\text{m}$, $20\,\mu\text{m}$, $10\,\mu\text{m}$, $5\,\mu\text{m}$, $2.5\,\mu\text{m}$, $1.25\,\mu\text{m}$, and lengths are $L = 40\,\mu\text{m}$, $10\,\mu\text{m}$, $4\,\mu\text{m}$, $2\,\mu\text{m}$, $1\,\mu\text{m}$. Digital decoding/selection circuitry is included in each cell and outside the array. Elements in the chip are arranged in a way such that all NMOS transistors have their drains connected to chip pin *DN*, all PMOS transistors have their drains connected to chip pin *DP*, all NMOS and PMOS transistors have their sources connected to chip pin *S*, all NMOS and PMOS transistors have their gates short-circuited to their sources, except for one NMOS-PMOS pair which has their gates connected to chip pin *G*. The digital bus and the internal decoding/selection circuitry selects one cell in the array and, inside this cell, one pair of NMOS and PMOS transistors, connecting their gates

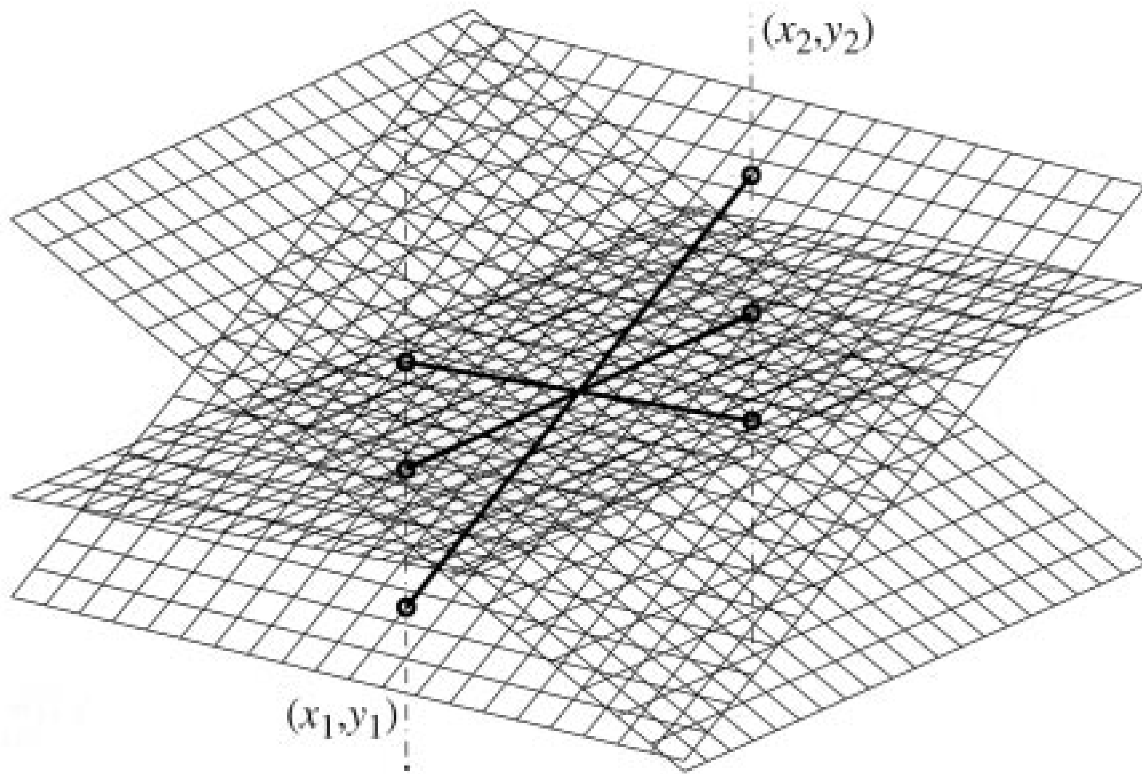

Fig. 1. Illustration of gradient-induced mismatch component for three different dies, each characterized by a gradient-plane.

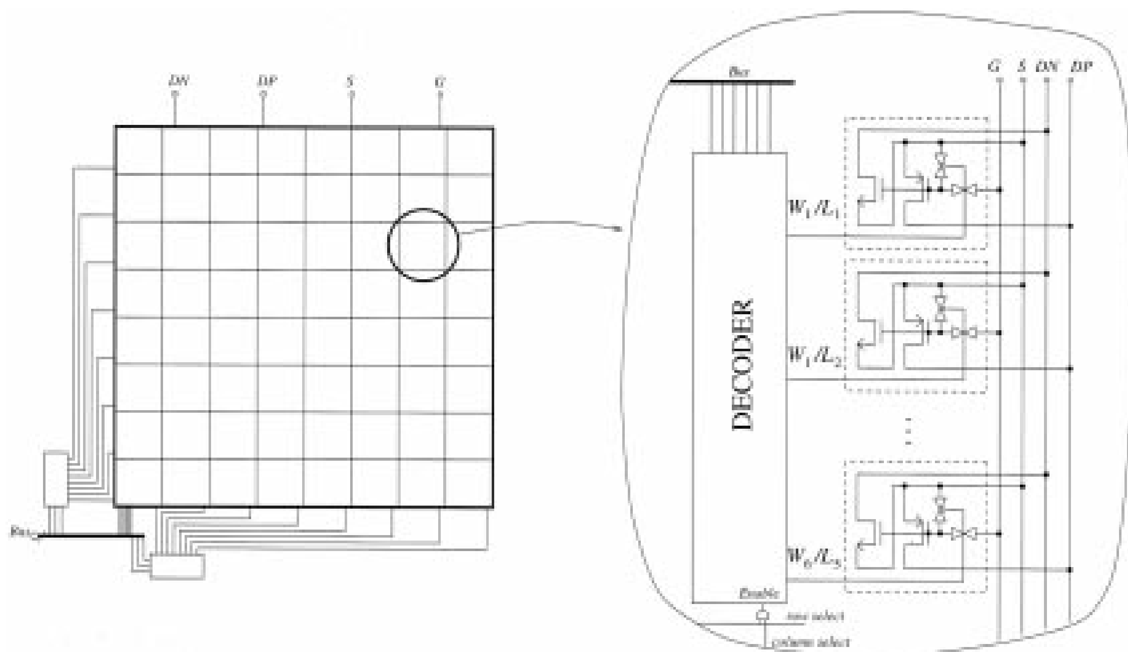

Fig. 2. Mismatch characterization chip simplified schematic.

to chip pin G. A chip with an 8×8 cell array has been fabricated in a digital $1.0\,\mu$m CMOS process which occupies an area of $4.0\,\text{mm} \times 3.5\,\text{mm}$, and uses 18 pins (12 for the decoding/selection *Bus*, *DN*, *DP*, *G*, *S*, V_{dd}, and *Gnd*). Cell size is $415\,\mu\text{m} \times 363\,\mu\text{m}$, so that distance between equal size transistors of adjacent cells is $363\,\mu$m. Some transistors in the periphery cells presented large systematic deviations with respect to those in the inside cells.[2] Consequently, statistical computations were performed only on inner cells transistors, thus rendering an effective cell array of 6×6. Note that, although the distance between equal transistors is fairly large ($363\,\mu$m), this distance does not contribute to the second term in equation (2) on our mismatch characterizations. The reason is, as discussed above, that the gradient contribution to ΔP is equal for all pairs (assuming gradients are defined by planes, which is a reasonable assumption for a die size of $3.5\,\text{mm} \times 4.0\,\text{mm}$) and is thus eliminated when computing[3] $\sigma_{(\Delta P)}$.

The experimental characterization set-up consists of a host computer controlling the decoding/ selection bus and a DC-curves measuring instrument (like the HP4145). This instrument is connected to pins *DN*, *DP*, *S*, *G*, and chip substrate. The host computer selects one NMOS-PMOS pair and the instrument measures first the NMOS transistor (putting connection *DP* into high-impedance and measuring through pins *S*, *G*, and *DN*) and then the PMOS transistor (putting connection *DN* into high-impedance and measuring through pins *S*, *G*, and *DP*). A simple software program sequentially selects and measures all transistors in the chip. Section 3 describes the DC-curves that were measured for each transistor, how electrical parameter mismatches were extracted from these curves, and how their statistical characterization was performed.

3. Mismatch Parameter Extraction and Statistical Characterization

Transistor parameter mismatches were obtained by measuring pairs of identical transistors located in adjacent cells of the same row. Since in the chip there are 6×6 effective cells, there are 6 rows, each of which provides 5 pairs of adjacent cells. This results in 30 adjacent transistor pairs (for each transistor size and type). The statistical significance of 30 measurements to determine a standard deviation is as follows: assuming a normal distribution, if 30 samples are available to compute a standard deviation $\sigma_{Computed}$, it can be assured that the 95% confidence interval for the real standard deviation σ_{Real} is [16]

$$0.7964 \times \sigma_{Computed} \leq \sigma_{Real} \leq 1.344 \times \sigma_{Computed} \qquad (3)$$

For each transistor pair, four curves were measured. Two of them while operating in the ohmic region and the other two for saturation (always in strong inversion). These curves are

$$\textbf{Curve 1:} \quad I_{DS}(V_{GS}) \quad , \quad V_{SB} = 0\,\text{V}, \quad V_{DS} = 0.1V \quad , \quad V_{GS} \in [1.5, 5.0] \qquad (4)$$

$$\textbf{Curve 2:} \quad I_{DS}(V_{SB}) \quad , \quad V_{GS} = 3.0\,\text{V}, \quad V_{DS} = 0.1\,\text{V} \quad , \quad V_{SB} \in [0, 2.0] \qquad (5)$$

$$\textbf{Curve 3:} \quad I_{DS}(V_{GS}) \quad , \quad V_{SB} = 0\,\text{V}, \quad V_{DS} = 4.0\,\text{V} \quad , \quad V_{GS} \in [1.5, 5.0] \qquad (6)$$

$$\textbf{Curve 4:} \quad I_{DS}(V_{SB}) \quad , \quad V_{GS} = 3.0\,\text{V}, \quad V_{DS} = 4.0\,\text{V} \quad , \quad V_{SB} \in [0, 2.0] \qquad (7)$$

Curves 1 and 3 are intended to characterize the current gain factor β, the voltage threshold V_{T0} and the mobility degradation parameter θ, while Curves 2 and 4 intend to characterize the bulk threshold parameter γ. Care must be taken in order to keep current levels sufficiently small so that mismatch introduced by series resistances (contact resistances, variable length routing wires, ...) is negligible. The following strong inversion large signal transistor model was assumed,[4]

$$I_{DS} = \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS}}{1 + \theta(V_{GS} - V_T(V_{SB}))} V_{DS}, \quad \text{for ohmic region (Curves 1, 2)} \qquad (8)$$

$$I_{DS} = \frac{\beta}{2} \frac{(V_{GS} - V_T(V_{SB}))^2}{1 + \theta(V_{GS} - V_T(V_{SB}))}, \quad \text{for saturation region (Curves 3, 4)} \qquad (9)$$

where,

$$V_T(V_{SB}) = V_{T0} + \gamma\left[\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right] \qquad (10)$$

Note that equation (9) is obtained from equation (8) by replacing V_{DS} by $V_{DS_{sat}} = V_{GS} - V_T(V_{SB})$. These curves depend nonlinearly on the *large signal*

parameters to be extracted ($\beta,\ V_{T0},\ \theta$ and γ) as well as on the measured data points $\{V_{GS}\}$ and $\{V_{SB}\}$. Therefore, these *large-signal parameters* should be extracted using nonlinear multi-parameters curve fitting techniques, such as the Levenberg- Marquadt method [17]. For a given transistor pair, the mismatch in the extracted *large-signal parameters* can be obtained directly by taking the parameters difference. However, *large-signal parameters* are always extracted with a certain error by whatever numerical algorithm is used. The reasons are noise present in the measured data (I_{DS}), limited number of data points measured, approximate nature of the mathematical nonlinear models (i.e equations (8)–(10)), among others. Consequently, it is much more reliable to fit the current mismatch data $\Delta I_{DS}/I_{DS}$ to its theoretical equation [9–11],

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \beta}\Delta\beta + \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_T}\left(\frac{\partial V_T}{\partial V_{T0}}\Delta V_{T0} + \frac{\partial V_T}{\partial \gamma}\Delta\gamma\right) + \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta}\Delta\theta \tag{11}$$

and extract from it the *mismatch parameters* $(\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta, \Delta\gamma)$ directly. In order to compute the different *mismatch parameter* coefficients in equation (11) the *large signal parameters* $(\beta, V_T, \theta, \gamma)$ are needed. Their values are now less critical, but are common for the two transistors. One can take either those values extracted for the first or the second transistor, or the mean of both. Depending on whether the transistors are operated in ohmic or saturation region, equation (11) changes as follows,

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} - \frac{1+\frac{1}{2}\theta V_{DS}}{[V_{GS}-V_T(V_{SB})-\frac{1}{2}V_{DS}][1+\theta(V_{GS}-V_T(V_{SB}))]}\Delta V_T - \frac{V_{GS}-V_T(V_{SB})}{1+\theta(V_{GS}-V_T(V_{SB}))}\Delta\theta \quad , \quad \text{for ohmic} \tag{12}$$

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} - \frac{2+\theta(V_{GS}-V_T)}{[V_{GS}-V_T(V_{SB})][1+\theta(V_{GS}-V_T(V_{SB}))]}\Delta V_T - \frac{V_{GS}-V_T(V_{SB})}{1+\theta(V_{GS}-V_T(V_{SB}))}\Delta\theta \quad , \quad \text{for saturation} \tag{13}$$

where,

$$\Delta V_T = \Delta V_{T0} + \Delta\gamma\left[\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right] \tag{14}$$

The *mismatch parameters* to be extracted from these equations would be $\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta$ and $\Delta\gamma$.

Since $\Delta I_{DS}/I_{DS}$ is obtained from two independent measurements of I_{DS}, it is important to assure that their measurement conditions are as similar as possible. This means that both curves should be measured as close as possible in time (i.e. consecutively) and that the settings of the instrument should not change in between. Thus the procedure should be as follows:

```
1. Go to next transistor pair
2. For curve = 1 to 4
     2.1. measure I_DS1 for 1st transistor
     2.2. measure I_DS2 for 2nd transistor
     2.3. compute '2⟨I_DS1 − I_DS2⟩/⟨I_DS1 + I_DS2⟩'
3. Go to Step 1
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Note that by this procedure the second transistor of a transistor pair is also the first transistor of the next transistor pair, and is therefore measured twice. However, in between, the settings of the instrument change (from Curve 1 to Curve 4) and little offsets might have been introduced.[5] An alternative could be to measure Curve 1 for all transistors, then Curve 2, and so on. But then, for a given transistor, there would be a large time between the measurement of the different curves, which could introduce an extra artificial mismatch due to, for example, temperature drift.

The precision with which the *mismatch parameters* are extracted depend on the number of data points measured for each curve, and on the precision with which each data point is measured. We noticed that using a large number of data points does not improve much the precision of the extracted parameters, and observed that a reasonable compromise between measurement-time and precision was obtained for 11 data points. On the contrary, it was very important to measure each data point with as much precision as possible, i.e. with as little measurement noise as possible. Instruments eliminate noise by repeating the measurement several times and providing the average as the result. In our case, we set the instrument to average 256 measurements. This way, when computing $\Delta I_{DS}/I_{DS}$, we do not obtain pure noise.

Regarding the large signal model, note that equations (8)–(10) describe a very simplistic MOS transistor model. This means that we cannot expect to obtain for all transistor sizes the same large signal

parameters. Furthermore, for the same transistor, we should not expect to obtain the same *large signal parameters* when it is biased in ohmic or in saturation. Consequently, for each transistor, the large signal parameters should be extracted independently for Curves 1–2 (equations (8) and (10)) and Curves 3–4 (equations (9) and (10)).

Regarding the mobility reduction parameter θ in equations (8)–(9), it is important to know that by these equations an effective θ_{eff} will be extracted that includes additional terms. In ohmic region, if one includes a drain series resistance R_D and a source series resistance R_S, replaces in equation (8) V_{GS} by $V_{GS} - R_S I_{DS}$ and V_{DS} by $V_{DS} - (R_S + R_D)I_{DS}$, and derives a closed form expression for I_{DS} after neglecting some terms, a similar equation to equation (8) results in which θ has been replaced by

$$\theta_{eff}\big|_{ohmic} = \theta + \beta R_S + \beta R_D \frac{V_{GS} - V_T - V_{DS}}{V_{GS} - V_T} \tag{15}$$

If $V_{DS} \ll V_{GS} - V_T$, then

$$\theta_{eff}\big|_{ohmic} \approx \theta + \beta(R_S + R_D) = \theta + 2\frac{\mu C_{ox} l_d R_\square}{L} \tag{16}$$

where $R_\square$ is the diffusion sheet resistance per square and l_d is the distance from the gate diffusion edge to the source (and drain) contact region. By evaluating the terms in equation (16) for typical parameter values, it can be seen that the second term can be of the order of θ, or larger for small values of L. As V_{DS} increases, the effect of R_D becomes weaker until it dissappears as the transistor enters saturation.

Another effect that influences the extracted value for θ_{eff} is the carriers velocity saturation ν_s, which can be expressed as [18–19]

$$\begin{aligned} I_{DS} &= \beta \frac{V_{GS} - V_T - \frac{1}{2}V_{DS}}{[1 + \theta(V_{GS} - V_T)]\left[1 + \frac{\mu}{2\nu_s L}V_{DS}\right]} V_{DS} \\ &\approx \beta \frac{V_{GS} - V_T - \frac{1}{2}V_{DS}}{1 + (V_{GS} - V_T)\left(\theta + \frac{\mu}{2\nu_s L}\frac{V_{DS}}{V_{GS} - V_T}\right)} V_{DS} \end{aligned} \tag{17}$$

for ohmic region, while for saturation V_{DS} is replaced by $V_{DS_{sat}} = V_{GS} - V_T$.

Consequently, including the effects of drain and source resistances, as well as carrier velocity saturation, results in the following θ_{eff} value,

$$\begin{aligned} \theta_{eff} &= \theta + \beta(R_D + R_S) \\ &\quad + \left(\frac{\mu}{2\nu_s L} - \beta R_D\right)\frac{V_{DS}}{V_{GS} - V_T} \end{aligned} \tag{18}$$

where V_{DS} is substituted by $V_{DS_{sat}} = V_{GS} - V_T$ when the transistor is biased in saturation. Replacing β, R_D and R_S by their respective expressions results in

$$\begin{aligned} \theta_{eff} &= \theta + 2\frac{\mu C_{ox} l_d R}{L} \\ &\quad + \frac{\mu}{L}\left(\frac{1}{2\nu_s} - C_{ox} l_d R_\square\right)\frac{V_{DS}}{V_{GS} - V_T} \end{aligned} \tag{19}$$

where one can see that the extra terms are significant for short channel transistors. From equations (18)–(19) we can express the mismatch in θ_{eff} as[6]

$$\Delta\theta_{eff} \approx \Delta\theta_o + \frac{V_{DS}}{V_{GS} - V_T}\Delta\theta_e \tag{20}$$

where $\Delta\theta_o$ is the θ_{eff} mismatch in ohmic region when $V_{DS} \approx 0V$ and $\Delta\theta_o + \Delta\theta_e$ is the corresponding mismatch for saturation region. Consequently, this fact forces us to extract $\Delta\theta_{eff}$ for ohmic region (preferably with $V_{DS} \approx 0$) as well as for saturation. On the other hand, *mismatch parameters* $\Delta\beta/\beta$, ΔV_{T0} and $\Delta\ \gamma$ should be the same for ohmic and saturation regions.[7] According to this discussion, the mismatch model considered for a transistor pair will be

$$\begin{aligned} \frac{\Delta I_{DS}}{I_{DS}} &= \frac{\Delta\beta}{\beta} \\ &\quad - \frac{1 + \frac{1}{2}\theta_{eff}V_{DS}}{\left[V_{GS} - V_T(V_{SB}) - \frac{1}{2}V_{DS}\right][1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))]}\Delta V_T \\ &\quad - \frac{V_{GS} - V_T(V_{SB})}{1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))}\Delta\theta_o, \quad \text{for ohmic with } V_{DS} \approx 0 \end{aligned} \tag{21}$$

$$\begin{aligned} \frac{\Delta I_{DS}}{I_{DS}} &= \frac{\Delta\beta}{\beta} \\ &\quad - \frac{2 + \theta_{eff}(V_{GS} - V_T)}{[V_{GS} - V_T(V_{SB})][1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))]}\Delta V_T \\ &\quad - \frac{V_{GS} - V_T(V_{SB})}{1 + \theta_{eff}(V_{GS} - V_T(V_{SB}))}(\Delta\theta_o + \Delta\theta_e), \quad \text{for saturation} \end{aligned} \tag{22}$$

$$\Delta V_T = \Delta V_{T0} + \Delta\gamma\left[\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right] \tag{23}$$

where the *large signal parameters* $\beta, V_{T0}, \theta_{eff}$ and γ are different for ohmic and saturation, but the *mismatch parameters* $\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e$ and $\Delta\gamma$ are unique for each transistor pair.

For each transistor pair, the measurement/extraction procedure is as follows.

1. Measure Curve 1 (equation (4)) for both transistors. Extract the *large signal parameters* $\{\beta, V_{T0}, \theta_{eff}\}_{ohmic}$.
2. Measure Curve 2 (equation (5)) for both transistors. Compute (by equation (8)),

$$V_T(V_{SB}) = V_{GS} + \frac{\frac{\beta}{2}V_{DS}^2 + I_{DS}}{\theta_{eff} I_{DS} - \beta V_{DS}} \tag{24}$$

(using for β and θ_{eff} the values extracted from Curve 1) and fit it to equation (10) (using for V_{T0} the value extracted from Curve 1), obtaining $\{\gamma, \phi\}_{ohmic}$.

3. Measure Curve 3 (equation (6)) for both transistors. Extract the *large signal parameters* $\{\beta, V_{T0}, \theta_{eff}\}_{sat}$.
4. Measure Curve 4 (equation (7)) for both transistors. Compute (by equation (9)),

$$V_T(V_{SB}) = V_{GS} - \frac{\theta_{eff} I_{DS}}{\beta}\left[1 + \sqrt{1 + \frac{2\beta}{\theta_{eff}^2 I_{DS}}}\right] \tag{25}$$

(using for β and θ_{eff} the values extracted from Curve 3) and fit it to equation (10) (using for V_{T0} the value extracted from Curve 3), obtaining $\{\gamma, \phi\}_{sat}$.

At this point we have the *large signal parameters* for ohmic $\{\beta, V_{T0}, \theta_{eff}, \gamma, \phi\}_{ohmic}$ and saturation $\{\beta, V_{T0}, \theta_{eff}, \gamma, \phi\}_{sat}$. To obtain now the five *mismatch parameters* $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$ for the transistor pair, the procedure continues as follows,

5. For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 1

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Curve1} = \frac{\Delta\beta}{\beta} + X_{1a}\Delta V_{T0} + X_{2a}\Delta\theta_o \tag{26}$$

compute the coefficients

$$X_{1a} = -\frac{1 + \frac{1}{2}\theta_{eff}V_{DS}}{\left[V_{GS} - V_{T0} - \frac{1}{2}V_{DS}\right][1 + \theta_{eff}(V_{GS} - V_{T0})]}$$

$$X_{2a} = -\frac{V_{GS} - V_{T0}}{1 + \theta_{eff}(V_{GS} - V_{T0})} \tag{27}$$

using $\{V_{T0}, \theta_{eff}\}_{ohmic}$.

6. For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 2

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Curve2} = \frac{\Delta\beta}{\beta} + X_{1b}\Delta V_{T0} + X_{2b}\Delta\theta_o + X_{3b}\Delta\gamma \tag{28}$$

compute the coefficients

$$X_{1b} = -\frac{1 + \frac{1}{2}\theta_{eff}V_{DS}}{\left[V_{GS0} - V_T(V_{SB}) - \frac{1}{2}V_{DS}\right][1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))]}$$

$$X_{2b} = -\frac{V_{GS0} - V_T(V_{SB})}{1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))}$$

$$X_{3b} = X_{1b}[\sqrt{\phi + V_{SB}} - \sqrt{\phi}] \tag{29}$$

using $\{\theta_{eff}, \phi\}_{ohmic}$, and where $V_{GS0} = 3.0\,\text{V}$ and $V_T(V_{SB})$ is obtained from equation (24).

7. For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 3

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Curve3} = \frac{\Delta\beta}{\beta} + X_{1c}\Delta V_{T0} + X_{2c}(\Delta\theta_o + \Delta\theta_e) \tag{30}$$

compute the coefficients

$$X_{1c} = -\frac{2 + \theta_{eff}(V_{GS} - V_{T0})}{(V_{GS} - V_{T0})[1 + \theta_{eff}(V_{GS} - V_{T0})]}$$

$$X_{2c} = -\frac{V_{GS} - V_{T0}}{1 + \theta_{eff}(V_{GS} - V_{T0})} \tag{31}$$

using $\{V_{T0}, \theta_{eff}\}_{sat}$.

8. For the current mismatch $\Delta I_{DS}/I_{DS}$ of Curve 4

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Curve4} = \frac{\Delta\beta}{\beta} + X_{1d}\Delta V_{T0} + X_{2d}(\Delta\theta_o + \Delta\theta_e) + X_{3d}\Delta\gamma \tag{32}$$

compute the coefficients

$$X_{1d} = -\frac{2 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))}{(V_{GS0} - V_T)[1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))]}$$

$$X_{2d} = -\frac{V_{CS0} - V_T(V_{SB})}{1 + \theta_{eff}(V_{GS0} - V_T(V_{SB}))}$$

$$X_{3d} = X_{1d}[\sqrt{\phi + V_{SB}} - \sqrt{\phi}] \tag{33}$$

using $\{\theta_{eff}, \phi\}_{sat}$, and where $V_{GS0} = 3.0\,\text{V}$ and $V_T(V_{SB})$ is obtained from equation (25).

9. Fit simultaneously equations (26), (28), (30) and (32) using the Least Squares Minimum (LSM) algorithm, obtaining the optimum five *mismatch parameters* $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$.

This measurement/extraction procedure is repeated for the $N_T = 30$ transistor pairs. For each extracted

mismatch parameter ΔP $(\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma)$ its standard deviation $\sigma_{(\Delta P)}$ is computed, as well as all correlations between pairs of *mismatch parameters* $r_{(\Delta P_1, \Delta P_2)}$. For each fabricated chip, standard deviations and correlations are obtained for each transistor size and type (NMOS and PMOS).

4. Characterization Results

A mismatch characterization chip was fabricated in a digital double-metal single-poly $1.0\,\mu$m CMOS process. The die area of the chip is $3.5\,\text{mm} \times 4.0\,\text{mm}$. Ten samples were delivered by the foundry, eight of which were fault free. For each fault free die, transistor size, and transistor type, the following standard deviations of the *mismatch parameters* were extracted, following the procedure described in the previous Section,

$$\sigma_{(\Delta\beta/\beta)}, \sigma_{(\Delta V_{T0})}, \sigma_{(\Delta\theta_o)}, \sigma_{(\Delta\theta_e)}, \sigma_{(\Delta\gamma)} \tag{34}$$

Also, their respective correlation terms were obtained

$$r_{(\Delta\beta,\Delta V_{T0})}, r_{(\Delta\beta,\Delta\theta_o)}, r_{(\Delta\beta,\Delta\theta_e)}, r_{(\Delta\beta,\Delta\gamma)}, r_{(\Delta V_{T0},\Delta\theta_o)}, \\ r_{(\Delta V_{T0},\Delta\theta_e)}, r_{(\Delta V_{T0},\Delta\gamma)}, r_{(\Delta\theta_o,\Delta\theta_e)}, r_{(\Delta\theta_o,\Delta\gamma)}, r_{(\Delta\theta_e,\Delta\gamma)} \tag{35}$$

Knowing these five standard deviations and ten correlation coefficients (for each transistor size and type), one should be able to predict the standard deviation of the measured current mismatch. This

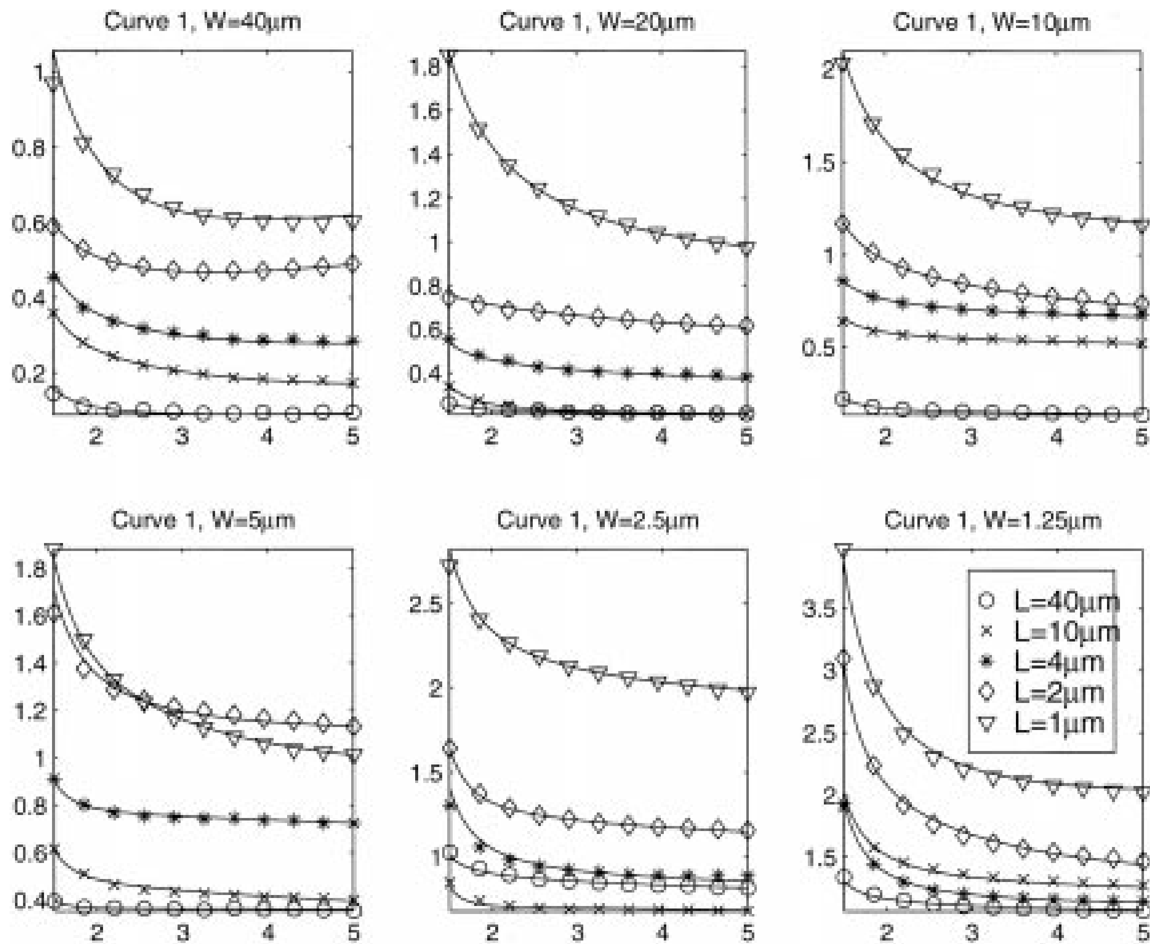

Fig. 3. Measured vs. predicted current mismatch $\sigma(\Delta I_{DS}/I_{DS})$ (in %) for Curve 1 for all transistor sizes for one of the chips. Horizontal scale is V_{GS} from 1.5 V to 5.0 V.

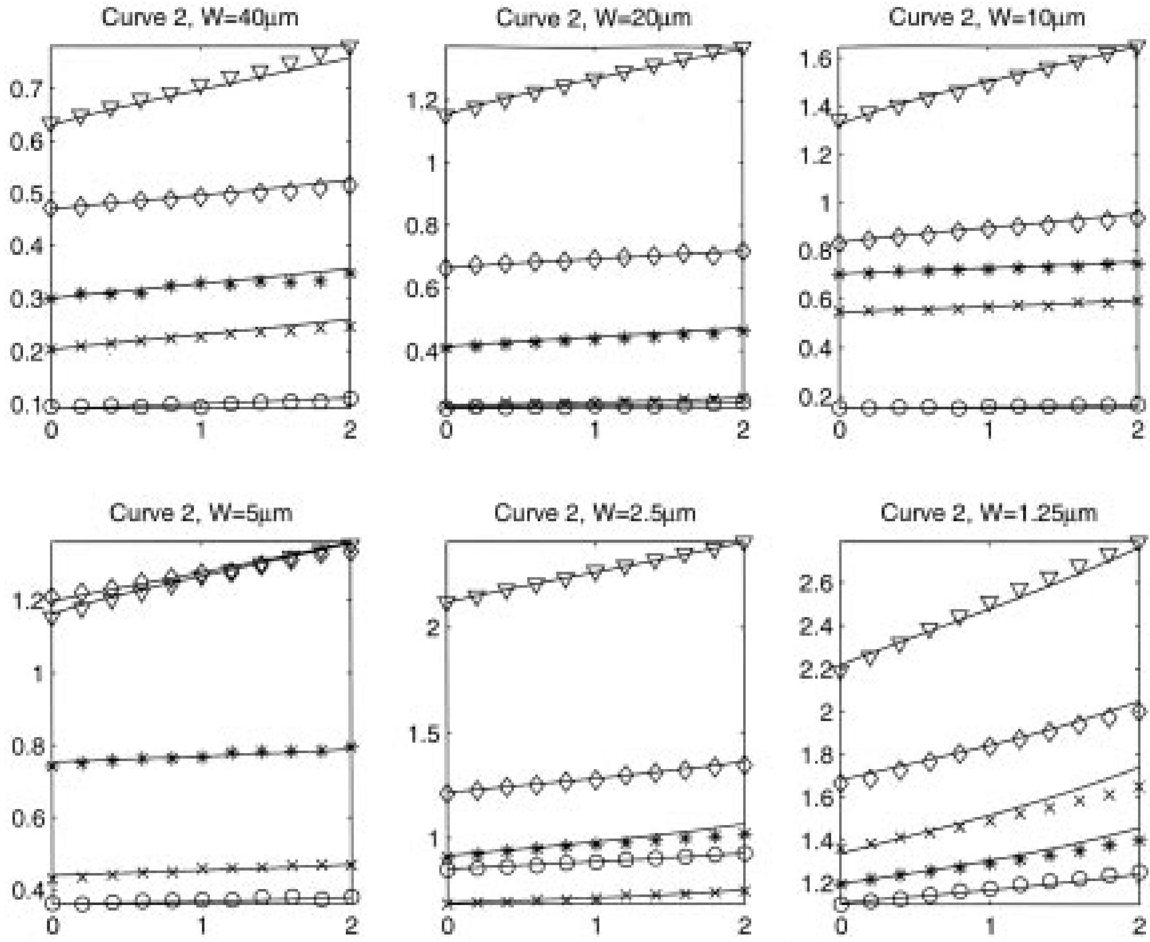

Fig. 4. Measured vs. predicted current mismatch $\sigma(\Delta I_{DS}/I_{DS})$ (in %) for Curve 2 for all transistor sizes for one of the chips. Horizontal scale is V_{SB} from 0 V to 2.0 V.

standard deviation can be obtained for example for Curve 1 from equation (26),

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right)\Big|_{\text{Curve1}} = \sigma^2_{\left(\frac{\Delta\beta}{\beta}\right)} + X_{1a}^2\sigma^2_{(\Delta V_{T0})} + X_{2a}^2\sigma^2_{(\Delta\theta_o)} + 2r_{(\Delta\beta,\Delta V_{T0})}X_{1a}\sigma_{\left(\frac{\Delta\beta}{\beta}\right)}\sigma_{(\Delta V_{T0})} + 2r_{(\Delta\beta,\Delta\theta_o)}X_{2a}\sigma_{\left(\frac{\Delta\beta}{\beta}\right)}\sigma_{(\Delta\theta_o)} + 2r_{(\Delta V_{T0},\Delta\theta_o)}X_{1a}X_{2a}\sigma_{(\Delta V_{T0})}\sigma_{(\Delta\theta_o)} \quad (36)$$

The right hand side of equation (36) can be obtained directly from the Curve 1 measured current mismatch values, and are shown in Fig. 3 with symbols (circles for $L = 40\,\mu$m, crosses for $L = 10\,\mu$m, stars for $L = 4\,\mu$m, diamonds for $L = 2\,\mu$m, triangles for $L = 1\,\mu$m) for all NMOS transistor sizes. The left hand side is computed using the extracted *statistical mismatch parameters* of equations (34)-(35) and the extracted *large signal parameters* for ohmic region, and is shown in Fig. 3 with continuous traces. In a similar way the measured and predicted current mismatches are shown for Curves 2, 3 and 4 in Fig. 4, Fig. 5, and Fig. 6, respectively. As can be seen, the agreement between measured and predicted current mismatch is excellent for all 4 curves, and for all transistor sizes including the minimum transistor length cases.

Fig. 3 to Fig. 6 correspond to the current mismatch measurements for one single chip, and the extracted *statistical mismatch parameters* for this same chip.

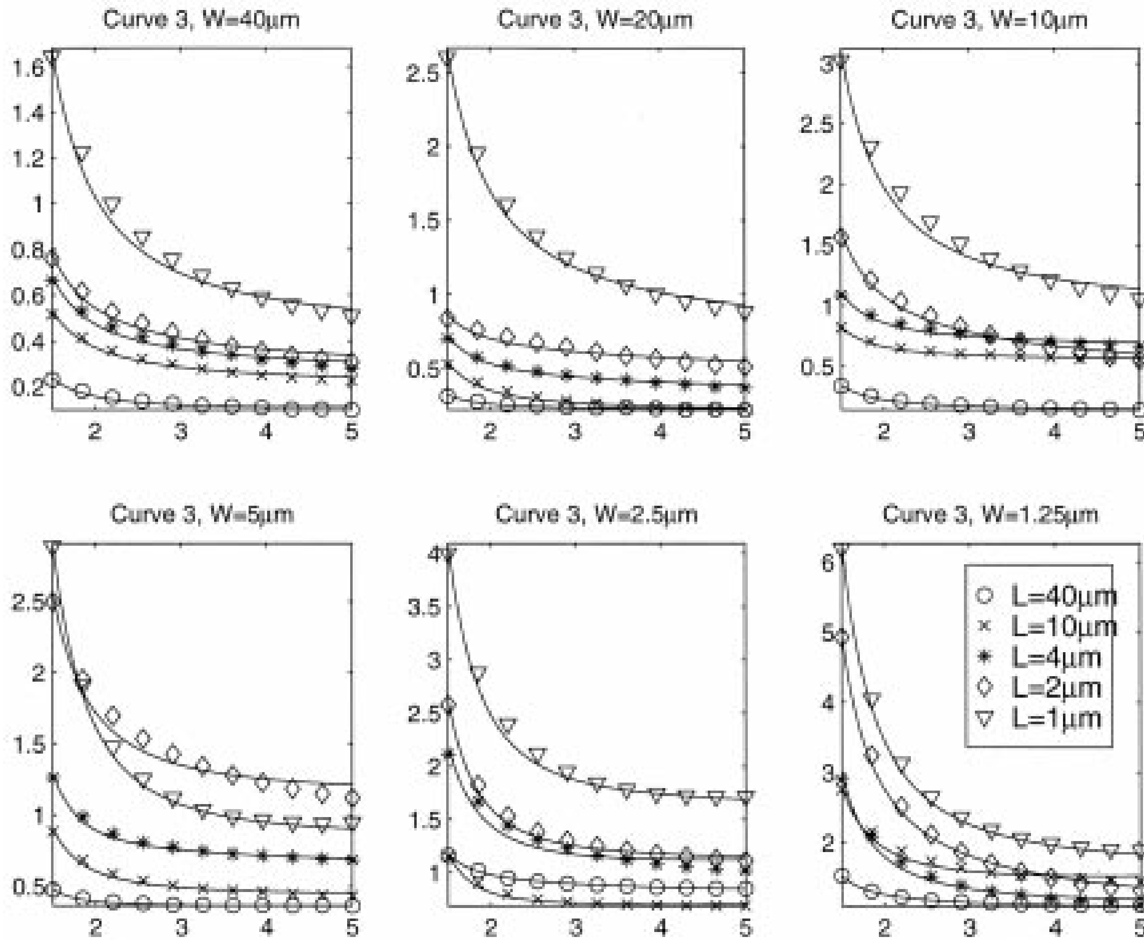

Fig. 5. Measured vs. Predicted Current Mismatch $\sigma(\Delta I_{DS}/I_{DS})$ (in%) for Curve 3 for all transistor sizes for one of the chips. Horizontal scale is V_{GS} from 1.5 V to 5.0 V.

When collecting the data for all eight measured chips, it becomes apparent that $\sigma(\Delta I_{DS}/I_{DS})$ changes from chip to chip. This is shown in Fig. 7 for the case of Curve 3, for all NMOS transistor sizes, where measured current mismatch is indicated with dots. Averaging over the eight chips the values of the extracted *statistical mismatch parameters* of equations (34–35), one predicts the central continuous line curves shown in Fig. 7. These predicted curves would characterize a ''*typical*'' or average mismatch, and their corresponding mismatch parameters can be called ''*typical case statistical mismatch parameters*''. If in Fig. 7 one focuses on the curves with maximum mismatch and takes the mismatch parameters for these curves only, they would correspond to a maximum mismatch case and could be called ''*maximum case statistical mismatch parameters*''. Similarly, focusing on curves with minimum mismatch and taking the mismatch parameters for these curves only, one could call them the ''*minimum case statistical mismatch parameters*''.[8] Providing this set of ''*typical*'', ''*maximum*'' and ''*minimum*'' statistical mismatch parameters for many transistor sizes, would characterize the transistor mismatch behavior as a function of transistor size.[9] The more dies are characterized, the more reliable would be the values for ''*typical*'', ''*maximum*'' and ''*minimum*'' statistical mismatch parameters for this technology. Following this procedure, we obtained for each transistor size and type, three values for each

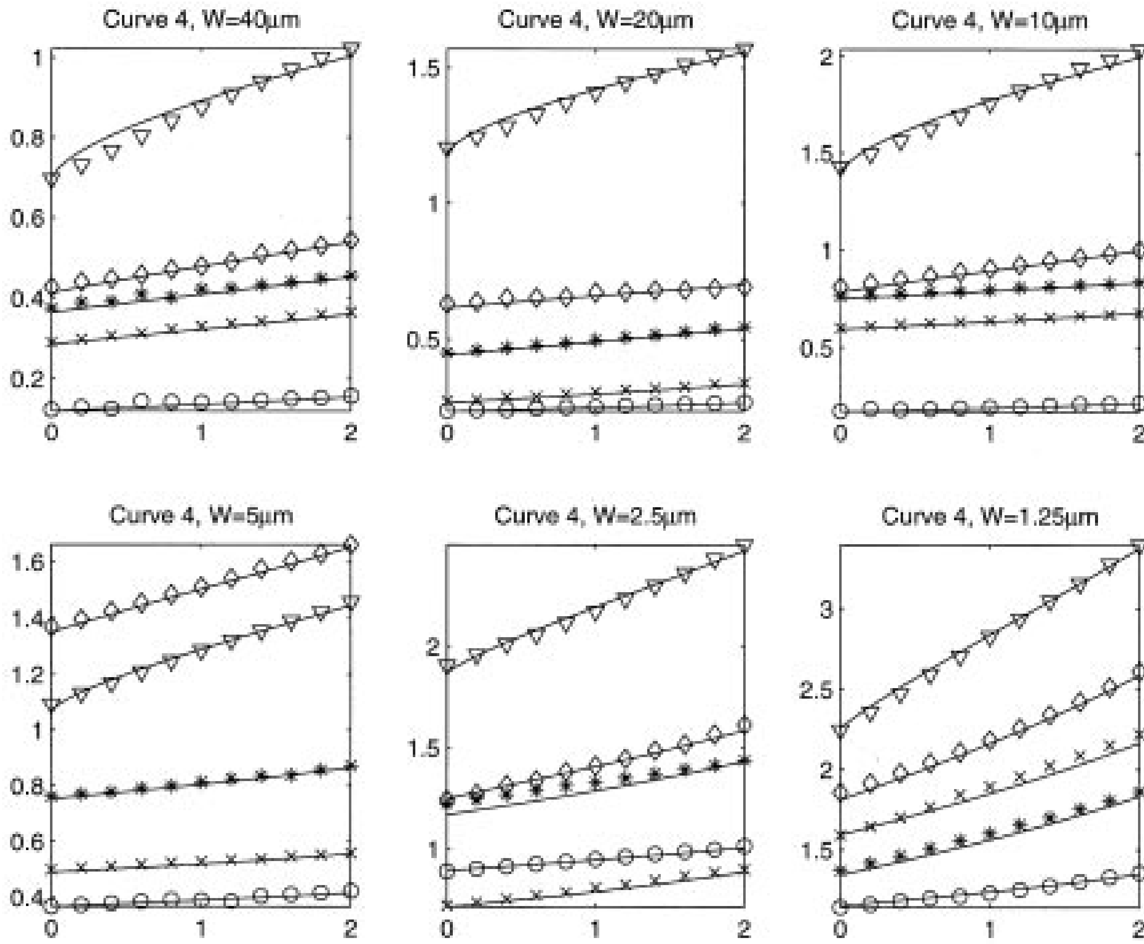

Fig. 6. Measured vs. predicted current mismatch $\sigma(\Delta I_{DS}/I_{DS})$ (in %) for Curve 4 for all transistor sizes for one of the chips. Horizontal scale is V_{SB} from 0 V to 2.0 V.

mismatch parameter (i.e., for the 5 standard deviations and for the 10 correlation coefficients): minimum, typical, and maximum values. The resulting values are shown in Table 2 for the 5 standard deviations and 3 of the correlations.

Noting the dispersion in standard deviation from chip to chip (see Fig. 7), one might reconsider, if it is strictly necessary to take into account all 5 standard deviations and all 10 correlations. Our experience is the following. If minimum transistor length is above 4 μm, $\Delta\theta_o$ and $\Delta\theta_e$ are not necessary to be extracted. One can extract $\Delta\beta/\beta$, ΔV_{T0} and $\Delta\gamma$ for each transistor pair. Furthermore, these 3 mismatch parameters can be extracted for only one region of operation (either ohmic or saturation) and still are able to predict the mismatch in the other region with acceptable precision. Even more, when predicting the mismatch in current, one can ignore the correlation terms and still predicted results are acceptable. This is what Pelgrom reported in 1989 [6], but for square transistors only.

The problems start when one wants to predict with good accuracy the mismatch for very small length transistors. In this case, $\Delta\theta_{eff}$ cannot be ignored, and since it is different for ohmic and saturation, mismatch parameters have to be extracted measuring both regions. However, when it comes to compute the current mismatch using the extracted deviations and correlations, we observed that many of the correlation terms can be ignored without loosing significant

Table 2. ''*Minimum*'', '*Typical*'' and ''*Maximum*'' statistical mismatch parameters for all transistor sizes, for NMOS transistors.

size	$\sigma(\frac{\Delta\beta}{\beta})$	$\sigma(\Delta V_{T0})$	$\sigma(\Delta\theta_o)$	$\sigma(\Delta\theta_e)$	$\sigma(\Delta\gamma)$	$r_{(\beta,\theta_o)}$	$r_{(\beta,\theta_e)}$	$r_{(\beta,\gamma)}$
40/40	0.0810,0.1180,0.1694	0.0598,0.0646,0.0776	0.0222,0.0260,0.0287	0.0179,00188,0.0192	0.0352,0.0352,0.0314	0.4271,0.5051,0.6804	−0.2972, 0.3495, 0567	−0.1968, −0.2374, −0.3696
40/10	0.1918,0.2450.04194	0.1027,0.1236,0.1212	0.0496,0.0576,0.0889	0.0356,0.0397,0.0405	0.0503,0.0577,0.0478	0.6057,0.7378,0.8332	−0.2102, −0.5005, −0.6913	−0.1621, −0.2125, −0.5127
40/4	0.2683,0.3527,0.4244	0.1439,0.1359,0.1265	0.0959,0.0862,0.0783	0.0695,0.0614,0.0669	0.0723,0.0768,0.0831	0.6515,0.5367,0.3581	−0.2497, −0.1187, 0.1266	−0.0749, −0.2864, −0.3366
40/2	0.5373,0.5934,0.6279	0.1806,0.1942,0.2260	0.1857,0.1842,0.1553	0.1230,0.1215,0.1335	0.1277,0.1092,0.1096	0.5293,0.5341,0.3237	0.5841,0.5067,0.3911	−0.3840, −0.4897, −03208
40/1	0.6267,0.7584,0.8375	0.5493,0.6268,0.7859	0.3526,0.3538,0.3764	0.7210,0.7066,0.7434	0.2455,0.3133,0.3414	0.6524,0.6417,0.6609	0.8200,0.8271,0.8992	−06582, −0.7859, −0.7804
20/40	0.1658,0.1918,0.2113	0.0782,0.0760,0.0754	0.0197,0.0218,0.0186	0.0189,0.0192,0.0171	0.0397,0.0430,0.0351	0.2855,0.3443,0.1590	0.0414,−0.1456, −0.3808	0.0932,−0.0295, −0.4844
20/10	0.2303,0.2673,0.3360	0.1463,0.1372,0.1174	0.0449,0.0449,0.0554	0.0346,0.0355,0.0333	0.0769,0.0751,0.0532	0.7144,0.6017,0.7676	−0.2081, −0.2085, −0.4159	0.00733,−0.0367, −0.3236
20/4	0.3644,0.4606,0.5686	0.1850,0.1725,0.1560	0.0808,0.0834,0.0655	0.0524,0.0538,0.0507	0.0912,0.1065,0.1276	0.6031,0.6339,0.6271	0.0620,−0.0796, −0.1890	−0.1515, −0.2618, −0.4155
20/2	0.8126,0.9192,1.2290	0.1924,0.2960,0.4021	0.1373,0.1381,0.1488	0.1495,0.1320,0.1593	0.0988,01630,0.2179	0.7223,0.7105,0.7578	0.6389,0.7157,0.7863	−0.4665, −0.5599, −0.7970
20/1	0.8938,1.1147,1.3062	0.6934,0.7396,0.8449	0.2820,0.2489,0.2250	0.7424,0.9097,0.9929	0.3523,0.3651,0.4469	0.6838,0.5797,0.3619	0.8393,0.8175,0.6900	−0.7940, −0.7681, −0.7915
10/40	0.1765,0.1782,0.2073	0.0959,0.0817,0.0973	0.0184,0.0215,0.0206	0.0222,0.0216,0.0237	0.0676,0.0584,0.0687	0.7076,0.4402,0.6649	0.2842,−0.2000, −0.5049	0.2715,−0.1412, −0.2373
10/10	0.4127,0.5073,0.5593	0.1563,0.1651,0.1601	0.0323,0.0416,0.0387	0.0441,0.0352,0.0305	0.1114,0.1013,0.1058	−0.0230, 0.2884, 0.4537	0.3193,0.1148, − 0.3376	0.1517,0.0833, − 0.2263
10/4	0.6109,0.7373,0.7455	0.1918,0.2214,0.2818	0.0803,0.0782,0.0633	0.0687,0.0634,0.0681	0.1556,0.1398,0.1522	0.3605,0.4906,0.1865	0.4287,0.2110,0.0825	−0.1299, −0.1419, −0.3573
10/2	0.7198,0.8354,0.8871	0.4525,0.4058,0.3665	0.1381,0.1470,0.1721	0.1374,0.1468,0.1392	0.1621,0.2108,0.2112	0.5985,0.6906,0.6331	0.6781,0.6971,0.5290	−0.3474, −0.3150, −0.4581
10/1	1.0877,1.2535,1.7232	0.8250,0.9211,1.2322	0.2423,0.2548,0.3388	0.8948,0.9791,1.2954	0.3721,0.4435,0.6520	0.4399,0.5019,0.5332	0.774,0.8078,0.9132	−0.6577, −0.7122, 0.8219
5/40	0.2914,0.3058,0.3540	0.1265,0.1130,0.1576	0.0362,0.0243,0.0174	0.0341,0.0289,0.0287	0.0922,0.0859,0.0857	0.4427,0.3751,0.6135	0.3313,−0.0608, −0.4809	0.2382,0.0695, − 0.3573
5/10	0.3457,0.4953,0.5421	0.2673,0.2513,0.2170	0.0547,0.0554,0.0566	0.0482,0.0501,0.0613	0.1436,0.1481,0.1586	0.4662,0.4937,0.3843	−0.2083, −0.1197, −0.2602	−0.0139, −0.0944, −0.4014
5/4	0.7238,0.7409,0.7766	0.3392,0.3974,0.4245	0.0947,0.0906,0.0879	0.0793,0.0877,0.1029	0.2296,0.2277,0.2651	0.7738,0.5399,0.5382	0.4719,0.2569, − 0.1194	0.3871,0.0243, − 0.0957
5/2	0.9226,1.0488,1.1640	0.3757,0.5146,0.6235	0.1457,0.1565,0.1398	0.1229,0.1572,0.1624	0.2599,0.2703,0.2552	0.6005,0.5356,0.3162	0.6524,0.4619,0.1655	−0.3118, −0.4077, −0.4313
5/1	1.2453,1.4932,1.7617	1.0856,1.1293,1.2046	0.2647,0.3388,0.3662	0.8270,1.1796,0.9461	0.3990,0.4434,0.4679	0.7244,0.6889,0.7209	0.2043,0.7908,0.7232	−0.1654, 0.4464, 0.4522
2.5/40	0.6463,0.7014,0.8769	0.1315,0.1621,0.1860	0.0341,0.0326,0.0380	0.0312,0.0393,0.0431	0.1224,0.1229,0.1319	0.3483,0.4687,0.6366	0.3620, −0.0296, −0.0151	0.0546, −0.2970, −0.2973
2.5/10	0.7914,0.9428,1.2220	0.3278,0.3352,0.3843	0.0773,0.0716,0.0746	0.0848,0.0805,0.0709	0.2187,0.2120,0.2021	0.5263,0.4433,0.4775	0.2621,0.0564,0.0886	0.0236, −0.1932, −0.0841
2.5/4	0.8265,0.9886,1.1443	0.4090,0.4867,0.4706	0.1199,0.1275,0.1093	0.1473,0.1251,0.0878	0.2557,0.3227,0.3218	0.5265,0.5107,0.2292	0.0147, −0.1128, 0.13134	0.1641, −0.1695, −0.1475
2.5/2	1.1947,1.5039,1.6513	0.6895,0.6886,0.8103	0.2712,0.2234,0.2577	0.1896,0.2236,0.2866	0.4770,0.4054,0.4264	0.6719,0.6035,0.4614	0.2481,0.3682,0.5227	−0.5052, −0.3380, −0.3817
2.5/1	1.5581,2.2289,2.8166	1.4730,1.4998,1.2860	0.4142,0.4484,0.4894	1.0709,1.2551,1.4136	0.6501,0.6728,0.6911	0.5358,0.6878,0.7717	0.6680,0.7376,0.7872	−0.5132, −0.4676, −0.6312
1.25/40	0.9465,1.1803,1.2577	0.2189,0.2209,0.2835	0.0431,0.0468,0.0449	0.0782,0.0677 0.0662,	0.2086,0.2100,0.2322	0.6666,0.4712,0.5014	−0.5220, −0.2806, −0.4813	−0.6209, −0.6295, −0.6965
1.25/10	1.0022,1.3116,1.5026	0.4266,0.4579,0.6131	0.0819,0.0978,0.1183	0.1188,0.1203,0.1124	0.2406,0.3352,0.3887	0.6077,0.4950,0.4826	0.0187, −0.3421, −0.3557	−0.2833, −0.4022, −0.4632
1.25/4	0.8918,1.1861,1.2925	0.6502,0.6167,0.6266	0.1813,0.1846,0.1894	0.1674,0.1724,0.1421	0.5101,0.4094,0.4367	0.2331,0.4218,0.6474	0.0369,0.0702, − 0.1827	−0.2527, −0.1290, −0.3595
1.25/2	1.5682,1.7683,2.3369	1.0032,1.0305,1.1551	0.2762,0.3012,0.2952	0.2499,0.2775,0.2808	0.4682,0.5661,0.6281	0.7386,0.6340,0.6216	0.5418,0.3916,0.5168	−0.0270, −0.1507, −0.3673
1.25/1	2.1338,2.3835,3.0209	1.6612,1.9373,2.0488	0.7417,0.5992,0.5728	1.0915,1.2876,1.4466	0.7702,0.8376,0.6368	0.7287,0.6989,0.7844	0.7344,0.7443,0.7502	−0.3454, −0.3964, −0.5105

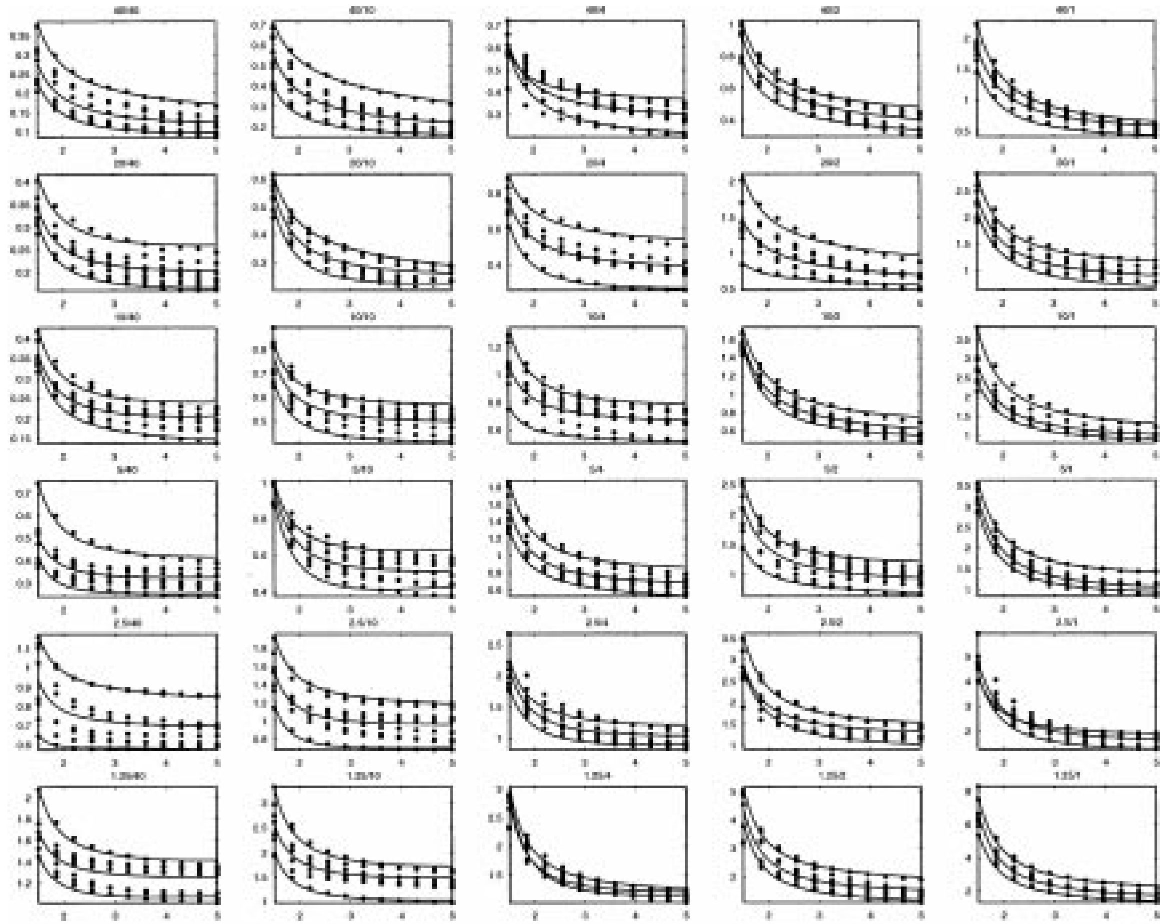

Fig. 7. Mismatches for Curve 3 for all 8 measured chips. Dots are measured $\sigma(\Delta I_{DS}/I_{DS})$ (in %), central continuous lines are predicted using extracted mismatch parameters averaged over all chips, top continuous lines correspond to chip with maximum mismatch, bottom continuous lines correspond to chip with minimum mismatch.

precision. According to our observations, only three correlation coefficients are needed to attain a good mismatch prediction: $r_{(\Delta\beta,\Delta\theta_o)}$, $r_{(\Delta\beta,\Delta\theta_e)}$ and $r_{(\Delta\beta,\Delta\gamma)}$. Fig. 8 illustrates all this for the most critical transistor size[10] ($W = 40\,\mu$m, $L = 2\,\mu$m), for Curves 1–4. Circles represent the measured current mismatch standard deviations. Continuous lines correspond to the case of extracting all 5 mismatch parameters and using all 5 standard deviations and all 10 correlation coefficients to predict current mismatch. The dashed line correspond to ignoring all correlation coefficients, except three: $r_{(\Delta\beta,\Delta\theta_o)}$, $r_{(\Delta\beta,\Delta\theta_e)}$, $r_{(\Delta\beta,\Delta\gamma)}$. The dashed-dotted lines correspond to extracting only $\Delta\beta/\beta$, ΔV_{TO} and $\Delta\gamma$, and ignoring all correlations among them. And finally, the dotted lines correspond to extracting $\Delta\beta/\beta$, ΔV_{TO} and $\Delta\gamma$ for ohmic region only and ignoring all correlations among them.

The set of ''*typical*'', ''*maximum*'' and ''*minimum*'' mismatch parameters (for standard deviations and correlations) for each size constitute the most precise and reliable mismatch characterization information we can provide for the measurement and characterization procedure we have used. However, this characterizes only a finite number of sizes. Linear interpolation could be used for obtaining the mismatch parameters for other sizes, or one can try to fit the data to some nonlinear function. This is precisely what we intend to do now. Table 1 shows

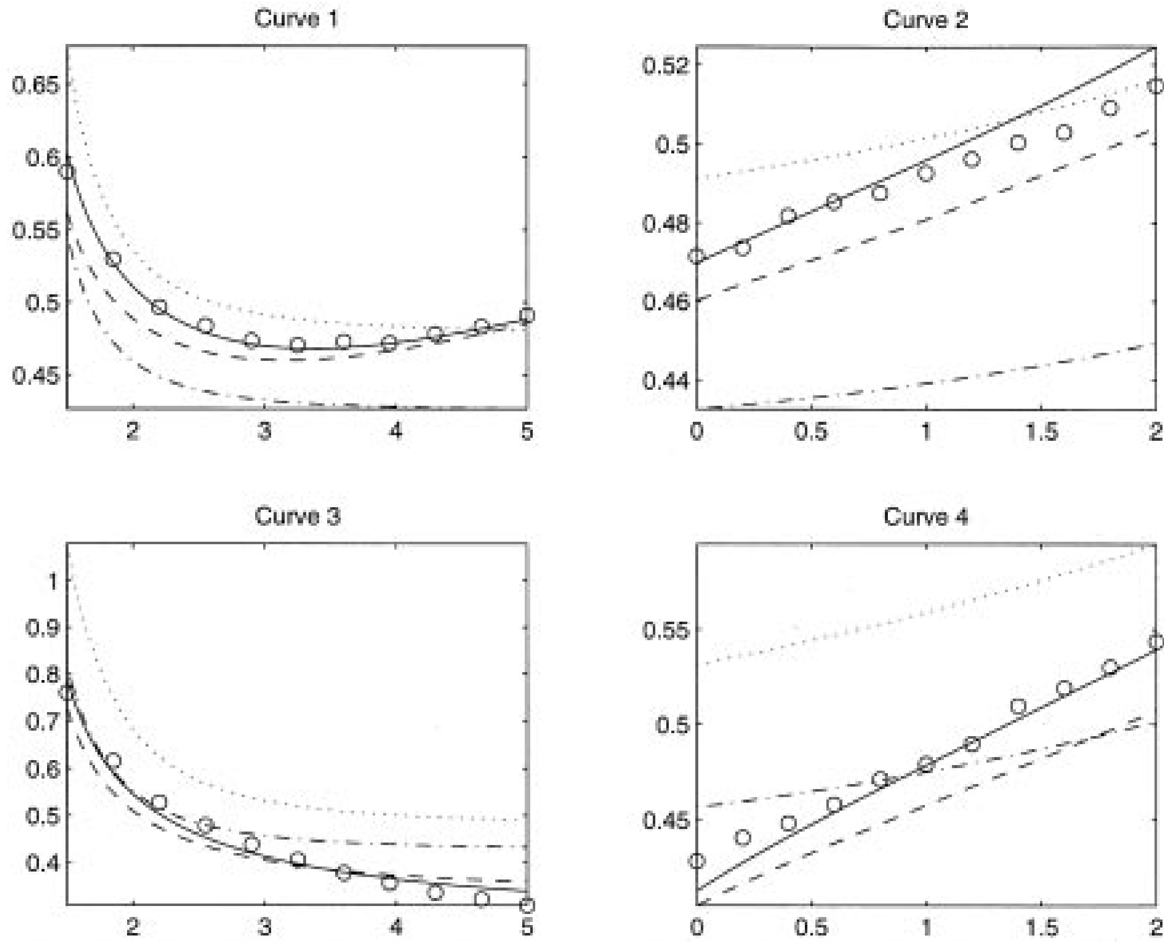

Fig. 8. Measured and predicted mismatch in current $\sigma(\Delta I_{DS}/I_{DS})$ (in %) for Curves 1–4 for transistor size $W = 40\,\mu$m, $L = 2\,\mu$m. Circles are measured mismatch. Continuous lines are predicted mismatches including all 5 standard deviations and all 10 correlation coefficients. Dashed lines are predicted mismatches using only the 3 most relevant correlation coefficients. Dashed-dotted lines correspond to the case of extracting only $\Delta\beta/\beta$, ΔV_{T0} and $\Delta\gamma$, and ignoring their correlation coefficients. Dotted lines correspond to extracting $\Delta\beta/\beta$, ΔV_{T0} and $\Delta\gamma$ for ohmic region only, and ignoring their correlation coefficients.

some of the dependencies on W and L that have been developed in the open literature for the standard deviations of mismatch parameters. As more precise mismatch models are developed, more terms are added to these functions based on interpretations of the underlying physical phenomena [10–11]. In the present study we just intend to obtain a mathematical function able to fit the measured data. We do not intend to provide a physical interpretation to the resulting fitting coefficients. Consequently, we selected a very general mathematical function and let the fitting routines select the best coefficients for our data. The chosen mathematical function is

$$\sigma^2{}_{(\Delta P)} = \sum_{m,n} \frac{C_{mn}}{(W - \varepsilon_w)^m (L - \varepsilon_l)^n} \tag{37}$$

where parameters C_{mn}, ε_w and ε_l are computed for each mismatch parameter ΔP. The results are shown in Fig. 9 for NMOS transistors. For example, Fig. 9(a) corresponds to *statistical mismatch parameter* σ $(\Delta\beta/\beta)$. Diamonds are the extracted values of σ $(\Delta\beta/\beta)$ for

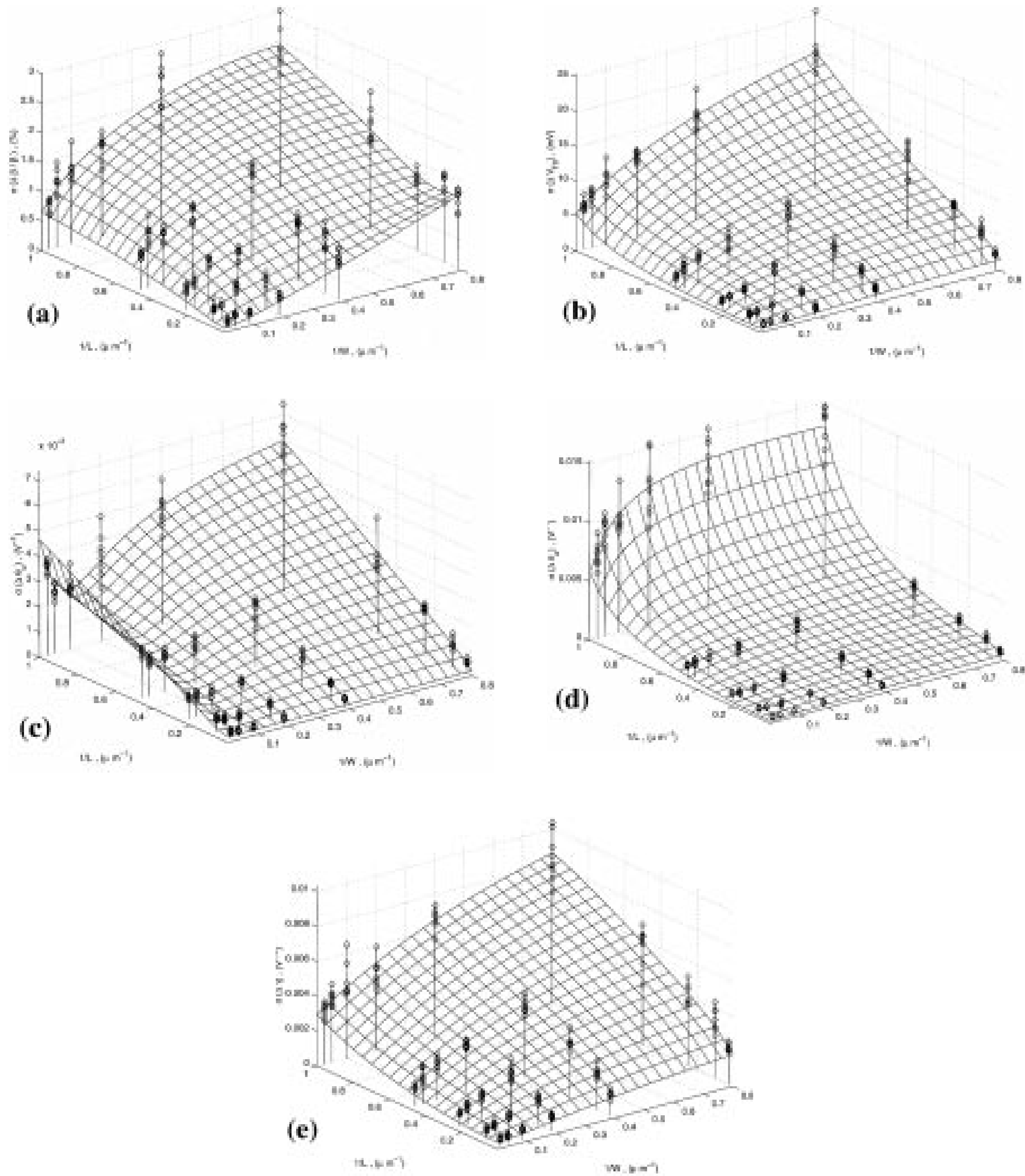

Fig. 9. Measured and fitted mismatch parameters for NMOS transistors. Diamonds are measured parameters for each transistor size and die. Surfaces correspond to fitted mathematical functions for (a) $\sigma(\Delta\beta/\beta)$, (b) $\sigma(\Delta V_{T0})$, (c) $\sigma(\Delta\theta_o)$, (d) $\sigma(\Delta\theta_e)$, (e) $\sigma(\Delta\gamma)$. Units for 1/W and 1/L axes are μm^{-1}.

each of the 30 transistor sizes, and for each of the 8 non-faulty measured chips. Using these 30×8 data points the surface in Fig. 9(a) is obtained, which is defined by the coefficients shown in Table 3, in the first row. The data was fitted using Least Mean Squares to minimize the error function

$$Error = \sum_{n_d}^{N_{dies}} \sum_{i}^{N_{sizes}} \omega_i [\sigma^2{}_{(\Delta P)}(W_i, L_i, n_d) - \sigma^2{}_{(\Delta P)_{fit}}(W_i, L_i, C_{nm}, \varepsilon_w, \varepsilon_l)]^2 \quad (38)$$

where $\sigma_{\Delta P}$ are the extracted standard deviations for each size and die, and $\sigma_{(\Delta P)_{fit}}$ is the function we want to fit by equation (37). Coefficients ω_i are weighting parameters for each transistor size defined as[11]

$$\omega_i = \frac{e^{-\Omega_i}}{\Omega_i^2} \quad (39)$$

where Ω_i characterizes the spread in $\sigma_{(\Delta P)}$ from die to die. This way transistor sizes whose inter-chip spread of $\sigma_{(\Delta P)}$ is large, contribute little to the error function in equation (38), while those with little inter-chip spread contribute with a stronger weight to this error.

The same procedure was applied for the other mismatch parameters. Fig. 9(b) shows the same for $\sigma_{(\Delta V_{T0})}$, Fig. 9(c) for $\sigma_{(\Delta \theta_o)}$, Fig. 9(d) for $\sigma_{(\Delta \theta_e)}$ and Fig. 9(e) for $\sigma_{(\Delta \gamma)}$. The corresponding fitted parameters $\{C_{mn}\}$, ε_w and ε_l are given in Table 3, where the coefficient units are such that in equation (37) W and L are expressed directly in μm. Note that the resulting surfaces in Fig. 9 are defined for the complete design space, whose limits are $1/W_{\max} = 0$ to $1/W_{\min} = 0.8\,\mu\text{m}^{-1}$ and $1/L_{\max} = 0$ to $1/L_{\min} = 1.0\,\mu\text{m}^{-1}$. At this point it is interesting to highlight that $\sigma_{(\Delta \theta_e)}$ depends mainly on L, and increases very rapidly for small values of L.

In the same manner the fitting surfaces and coefficients have been obtained for the standard deviations, the same procedure can be followed for the correlation coefficients. The resulting fitting coefficients are also given in Table 3. Note that now parameter ε_w and ε_l were not necessary to obtain a good fit.

By repeating everything for PMOS transistors, the resulting fitting parameters $\{C_{mn}\}$, ε_w and ε_l shown in Table 4 result.

5. Verification of Characterization Results

One can think of many ways of trying to verify the correctness and robustness of the experimentally extracted transistor mismatch statistical results. In this Section we describe a few ways that can help to achieve this goal.

A. *Precision Test*

A first indication that one might be on the good way is by measuring one chip without changing the transistor pair, and follow the same parameter extraction procedure and consequent statistical characterization. For example, in our chips we measured for each transistor size and type 30 different transistor pairs. If we just measure for each transistor size and type the same pair but 30 times, and follow the same mathematical procedures, we would extract a set of standard deviations and correlation coefficients that would give us the precision of our instruments and mathematical algorithms. When measuring the parameter P mismatch between two transistors the resulting measured ΔP value has two components,

$$\Delta P = \Delta P_{Real} + \Delta P_{meas} \quad (40)$$

where ΔP_{Real} is the real mismatch in parameter P between both transistors and ΔP_{meas} is an error component introduced by the measurement set-up and parameter extraction procedure. By repeating many measurements the quadratic deviations for equation (40) can be written as

$$\sigma^2_{(\Delta P)} = \sigma^2_{(\Delta P_{real})} + \sigma^2_{(\Delta P_{meas})} \quad (41)$$

because the random transistor mismatch and the measurement error are supposed to be uncorrelated. The values of $\sigma_{(\Delta P)}$ are given in Table 2, while those for $\sigma_{(\Delta P_{meas})}$ resulted to be less than 1/3 of those in Table 2 in the worst case, and were normally below 1/10. According to equation (41) it would be possible to compute the values for $\sigma_{(\Delta P_{Real})}$. However, let us say a few words on confidence intervals. If N_T is the number of measurements of a normally distributed random variable, and these measurements are used to compute a standard deviation for this variable, $\sigma_{computed}$, then there is a confidence interval for the real standard deviation σ_{Real} [13]

Table 3. Resulting fitted parameters for surfaces defined by equation (37) for NMOS transistors.

	C_{00}	C_{10}	C_{01}	C_{11}	C_{20}	C_{02}	C_{21}	C_{12}	C_{22}	ε_w	ε_l
$\sigma(\Delta\beta/\beta)$	4.73e − 07	0	0	1.11e − 03	2.14e − 04	1.57e − 04	−1.99e − 03	2.19e − 03	7.78e − 04	1.38e − 01	−9.32e − 01
$\sigma(\Delta V_{T0})$	3.49e − 07	0	0	1.85e − 04	1.13e − 05	1.21e − 06	2.46e − 04	−1.77e − 05	−1.84e − 05	−1.06e + 00	7.94e − 01
$\sigma(\Delta\theta_o)$	4.88e − 08	0	0	−5.87e − 06	−5.16e − 07	2.41e − 05	2.38e − 04	−5.88e − 04	4.64e − 03	−5.74e + 00	−5.13e − 02
$\sigma(\Delta\theta_e)$	5.48e − 08	0	0	−4.76e − 06	2.50e − 06	1.03e − 06	8.25e − 05	3.10e − 05	−7.03e − 05	−2.12e + 00	8.26e − 01
$\sigma(\Delta\gamma)$	1.53e − 07	0	0	3.19e − 05	1.68e − 05	1.73e − 06	1.97e − 04	−2.40e − 07	−5.39e − 05	−1.06e + 00	5.50e − 01
$r(\beta, V_{T0})$	−2.86e − 01	2.02e + 00	5.53e − 01	−7.41e + 00	−2.58e + 00	−9.88e − 01	1.04e + 01	7.91e + 00	−1.01e + 01	0	0
$r(\beta, \theta_o)$	5.28e − 01	−5.62e − 01	6.54e − 01	−7.97e − 01	5.83e − 01	−6.07e − 01	4.95e − 01	1.74e + 00	−1.34e + 00	0	0
$r(\beta, \theta_e)$	−6.18e − 01	2.30e + 00	3.63e + 00	−1.04e + 01	−2.54e + 00	−2.17e + 00	1.03e + 01	7.79e + 00	−7.52e + 00	0	0
$r(\beta, \gamma)$	−1.03e − 01	4.69e − 01	−6.21e − 01	−1.24e + 00	−1.46e + 00	−1.03e − 01	5.94e + 00	2.19e + 00	−5.61e + 00	0	0
$r(V_{T0}, \theta_o)$	−4.94e − 01	3.77e + 00	1.38e + 00	−9.64e + 00	−3.83e + 00	−1.33e + 00	1.04e + 01	9.31e + 00	−1.01e + 01	0	0
$r(V_{T0}, \theta_e)$	8.08e − 01	−8.30e − 01	−1.97e + 00	6.00e + 00	8.98e − 01	6.68e − 01	−5.85e + 00	−3.73e + 00	4.03e + 00	0	0
$r(V_{T0}, \gamma)$	6.65e − 01	−6.02e − 01	−5.45e − 01	3.44e + 00	6.46e − 01	7.26e − 01	−3.91e + 00	−4.65e + 00	5.04e + 00	0	0
$r(0_o, 0_e)$	−9.81e − 01	4.55e + 00	1.58e + 00	−1.07e + 00	−4.67e + 00	1.38e − 02	8.68e − 01	−2.66e + 00	2.83e + 00	0	0
$r(\theta_o, \gamma)$	−2.38e − 01	2.22e + 00	4.16e − 01	−3.76e + 00	−2.38e + 00	−7.19e − 01	4.59e + 00	3.60e + 00	−4.12e + 00	0	0
$r(\theta_e, \gamma)$	7.38e − 01	1.41e − 03	−1.79e + 00	4.41e + 00	−1.40e − 01	4.43e − 01	−3.50e + 00	−3.40e + 00	3.23e + 00	0	0

Table 4. Resulting fitted parameters for surfaces defined by equation (37) for PMOS transistors.

	C_{00}	C_{10}	C_{01}	C_{11}	C_{20}	C_{02}	C_{21}	C_{12}	C_{22}	ε_w	ε_l
$\sigma(\Delta\beta/\beta)$	1.61e − 06	0	0	1.09e − 03	1.72e − 04	1.30e − 04	−1.31e − 03	3.14e − 03	−5.35e − 04	2.92e − 01	−8.56e − 01
$\sigma(\Delta V_{T0})$	1.10e − 06	0	0	3.89e − 04	1.04e − 05	5.03e − 07	−2.13e − 04	−2.15e − 05	1.23e − 05	2.61e − 01	9.27e − 01
$\sigma(\Delta\theta_o)$	6.93e − 08	0	0	3.29e − 05	1.17e − 06	7.99e − 08	3.00e − 05	−1.82e − 06	−2.82e − 06	−2.73e − 01	9.16e − 01
$\sigma(\Delta\theta_e)$	5.59e − 09	0	0	2.39e − 05	5.86e − 06	1.71e − 06	7.75e − 05	1.51e − 05	−4.91e − 05	−9.87e − 01	5.70e − 01
$\sigma(\Delta\gamma)$	1.04e − 07	0	0	5.81e − 05	2.70e − 07	4.17e − 06	−1.37e − 05	1.02e − 08	−4.07e − 07	9.19e − 01	3.33e − 01
$r(\beta, v_{T0})$	6.70e − 02	1.31e + 00	−2.46e − 01	−4.09e + 00	−2.17e + 00	−1.60e − 01	7.45e + 00	4.65e + 00	−6.93e + 00	0	0
$r(\beta, \theta_o)$	5.85e − 01	−4.88e − 01	−2.47e − 03	2.72e + 00	8.84c − 01	−4.61e − 01	−3.17e + 00	−5.89e − 01	1.11e + 00	0	0
$r(\beta, \theta_e)$	2.55e − 01	−4.86e − 01	−1.92e + 00	3.34e + 00	−6.64e − 02	2.07e + 00	−3.21e + 00	−2.60e + 00	2.67e + 00	0	0
$r(\beta, \gamma)$	4.36e − 01	−1.08e + 00	−1.98e + 00	6.05e + 00	−1.35e − 01	9.61e − 01	−2.65e + 00	−4.22e + 00	2.17e + 00	0	0
$r(V_{T0}, \theta_o)$	2.17e − 01	1.84e + 00	1.38e − 01	−6.57e + 00	−2.78e + 00	4.56e − 01	9.12e + 00	4.09e + 00	−5.93e + 00	0	0
$r(V_{T0}, \theta_e)$	6.04e − 01	−7.42e − 01	−1.60e + 00	1.55e + 00	9.03e − 01	1.66e + 00	−2.41e + 00	−2.12e + 00	2.76e + 00	0	0
$r(V_{T0}, \gamma)$	3.96e − 01	3.73e − 01	−6.55e − 01	−1.86e + 00	−4.48e − 02	9.98e − 01	1.43e + 00	−8.49e − 01	8.96e − 01	0	0
$r(\theta_o, \theta_e)$	1.58e − 01	3.83e − 02	−2.18e + 00	−1.47e + 00	−9.41e − 01	2.88e + 00	3.14e + 00	−2.81e − 02	−1.20e + 00	0	0
$r(\theta_o, \gamma)$	4.77e − 01	7.95e − 01	−1.77e + 00	−1.56e + 00	−2.26e + 00	1.93e + 00	5.89e + 00	−1.58e + 00	−1.65e + 00	0	0
$r(\theta_e, \gamma)$	5.39e − 01	2.98e − 01	1.05e − 01	8.99e − 01	−1.63e − 01	−6.59e − 02	−1.74e + 00	−2.96e + 00	3.80e + 00	0	0

$$r_L(N_T) \times \sigma_{computed} \le \sigma_{Real} \le r_H(N_T) \times \sigma_{computed}. \quad (42)$$

Equation (3) gave the 95% confidence interval when $N_T = 30$ ($r_L \cong 0.8$, $r_H \cong 1.3$). In our case $\sigma_{(\Delta P)}$ and $\sigma_{(\Delta P_{meas})}$ have been obtained by $N_T = 30$ measurements, and consequently their 95% confidence interval is given by equation (3). On the other hand, we can define a (conservative) confidence interval for $\sigma_{(\Delta P_{Real})}$ which depends on those for $\sigma_{(\Delta P)}$ and $\sigma_{(\Delta P_{meas})}$,

$$\begin{aligned}(r_H^*)^2 \times \sigma^2_{(\Delta P_{Real})} &= \max[\sigma^2_{(\Delta P_{Real})}] = \max\{\sigma^2_{(\Delta P)}\} \\ &\quad - \min\{\sigma^2_{(\Delta P_{meas})}\} = r_H^2(N_T) \times \sigma^2_{(\Delta P)} \\ &\quad - r_L^2(N_T) \times \sigma^2_{(\Delta P_{meas})} \\ (r_L^*)^2 \times \sigma^2_{(\Delta P_{Real})} &= \min[\sigma^2_{(\Delta P_{Real})}] = \min\{\sigma^2_{(\Delta P)}\} \\ &\quad - \max\{\sigma^2_{(\Delta P_{meas})}\} = r_L^2(N_T) \times \sigma^2_{(\Delta P)} \\ &\quad - r_H^2(N_T) \times \sigma^2_{(\Delta P_{meas})} \end{aligned} \quad (43)$$

By defining

$$\alpha = \frac{\sigma_{(\Delta P_{meas})}}{\sigma_{(\Delta P)}} \quad (44)$$

it follows that

$$\begin{aligned} r_H^*(N_T) &= \sqrt{\frac{r_H^2(N_T) - \alpha^2 r_L^2(N_T)}{1-\alpha^2}} \\ r_L^*(N_T) &= \sqrt{\frac{r_L^2(N_T) - \alpha^2 r_H^2(N_T)}{1-\alpha^2}} \end{aligned} \quad (45)$$

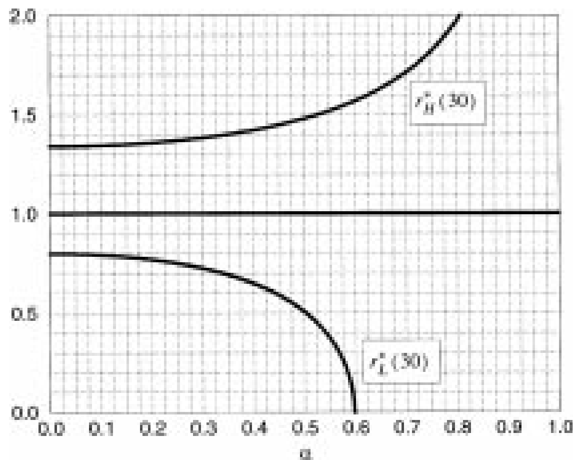

Fig. 10. Derived confidence interval for $\sigma_{(\Delta P_{Real})}$ as a function of $\alpha = \sigma_{(\Delta P_{meas})}/\sigma_{(\Delta P)}$, for $N_T = 30$.

Fig. 10 depicts the values of r_H^* and r_L^* as a function of α when $N_T = 30$. Note that even for values of α as high as 0.5 there is still a reasonable confidence interval for $\sigma_{(\Delta P_{Real})}$ (approximately $\pm 50\%$).

Since, in our case, the worst case α is less than 1/3, by Fig. 10 we can see that for this worst case, the confidence interval is not significantly degraded. Therefore, Table 2 provides confident enough values. This kind of precision test is also called in the literature *repeatability study* [10–11].

By this *repeatability study*, the only thing one can conclude is that whatever has been measured and given in Table 2, has been measured with acceptable precision. But this does not assure us that what is given in Table 2 is a good measurement of the physical quantities $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$, $\sigma_{(\Delta\theta_o)}$, $\sigma_{(\Delta\theta_e)}$, $\sigma_{(\Delta\gamma)}$ and respective correlations. To verify this other tests need to be performed.

B. Predicting $\sigma_{(\Delta I_{DS}/I_{DS})}$ of the Measured Curves

This is precisely what we did in Section 4 and showed in Figs. 3–6. Measured values of $\sigma_{(\Delta I_{DS}/I_{DS})}$ were compared against computed values of $\sigma_{(\Delta I_{DS}/I_{DS})}$ using the extracted mismatch parameters and equations of the type of equation (36). Figs. 3–6 show excellent agreement between measured and computed standard deviations[12].

This is already a very good indication that we are extracting correct enough mismatch parameters, because we are obtaining for each transistor pair a unique set of five mismatch parameters $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$ for all four measured curves. Since we had 30 pairs (for each size and type), it results in 50×30 mismatch parameters. Their statistical characterization yields 5 standard deviations and 10 correlation coefficients, which are the ones used to compute the continuous trace curves in Figs. 3–6.

However, here we are predicting the same curves we used to extract the mismatch parameters. A more severe test would be to predict other curves, obtained under different bias conditions. This is the test described next.

C. Predicting Differential Pairs Offset Voltage

Another good way to verify the degree of correctness of the extracted statistical mismatch parameters is to

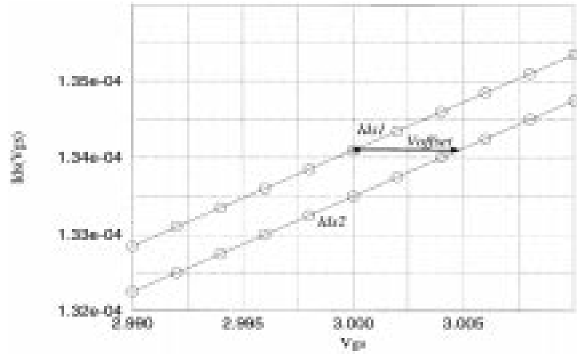

Fig. 11. Differential pair input offset voltage measurement. Curve I_{ds1} is for one of the transistors and I_{ds2} is for the other. Circles are experimentally measured points, lines are interpolated curves. Transistors are NMOS of size $40\,\mu\text{m} \times 40\,\mu\text{m}$.

use them to predict the offset voltage of differential pairs. In order to obtain direct measurements of differential pairs input voltage offset we used our mismatch characterization chip as follows. For each pair of transistors we measured the following curve

$$I_{DS}(V_{GS}) \quad , \quad V_{SB} = cte \quad , \quad V_{DS} = 3.0\,\text{V} \quad , \quad V_{GS} \in [2.99\,\text{V}, 3.01\,\text{V}] \qquad (46)$$

once for each transistor of the pair. Fig. 11 shows the measured points for one pair of NMOS transistors of size $40\,\mu\text{m} \times 40\,\mu\text{m}$. Also shown in Fig. 11 are the corresponding interpolated lines of the measurements

$$\begin{aligned} I_{DS1}(V_{GS}) &= m_1 V_{GS} + n_1 \\ I_{DS2}(V_{GS}) &= m_2 V_{GS} + n_2 \end{aligned} \qquad (47)$$

Consequently, the offset voltage for this differential pair is given by

$$V_{offset} = \frac{m_1 - m_2}{m_2} 3.0\,\text{V} + \frac{n_1 - n_2}{m_2} \qquad (48)$$

For each pair of transistors the curves of equation (46) were measured for two different values of V_{SB}. First for $V_{SB} = 0\,\text{V}$ (no substrate effect), and second for $V_{SB} = 1\,\text{V}$ (with substrate effect: $\Delta\gamma$ is affecting the offset voltage). These two offset voltages were measured for all transistor pairs, for all sizes for one of the dies. The standard deviation for these offset voltages was computed for each transistor size. Table 5, under the columns named ''Measured'', indicates the measured values for $\sigma_{(V_{offset})}$ as a function of transistor size and type.

In order to predict the standard deviation of this offset voltage using the extracted mismatch data of Table 2, note that (see Fig. 11)

$$V_{offset} = \frac{\Delta I_{DS}}{g_m} \quad \Rightarrow \quad \sigma_{(V_{offset})} = \frac{I_{DS}}{g_m} \sigma_{(\Delta I_{DS}/I_{DS})} \qquad (49)$$

where $\sigma_{(\Delta I_{DS}/I_{DS})}$ can be computed by evaluating an equation of the type of equation (36) but in saturation, and I_{DS}/g_m can be calculated using the mean extracted large signal parameters ($\overline{\beta}$, $\overline{V_{T0}}$, $\overline{\theta}$, and $\overline{\gamma}$). The values of $\sigma_{(V_{offset})}$ computed this way are also shown in Table 5 under the columns named ''Computed''. Note that the computed values stay within the confidence intervals of the measured values.

6. Mismatch Simulation using Conventional Electrical Circuit Simulators

Electrical circuit simulations using HSPICE have been performed in order to predict the measured differential pairs input offset voltages of Table 5. We describe two methods, both based on Monte Carlo simulations.

A. *Method 1*

In this method the idea is to use the transistor model provided by the manufacturer and introduce into it random variations for some of the most mismatch sensitive parameters. In our case, the manufacturer model is a Level 6 Hspice model. Obviously the physical meaning of the large signal parameters (such as β, V_{T0}, θ and γ) is different than for the simple model we assumed during our mismatch characterizations (equations (8)–(10)). Also, the manufacturer provides a size-independent model which is a good compromise for all sizes, while we obtained large signal parameters for each size (and region of operation). Besides this, and in our particular case, the manufacturer model does not include explicitly the mobility degradation parameter ''θ''. Consequently, we will not implement our 5-parameter mismatch model in this case (5 deviations and 10 correlations), but we will use only $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$ and $\sigma_{(\Delta\gamma)}$ and ignore all correlations (this corresponds to the dotted line cases in Fig. 8). The way to use this mismatch model in (H)Spice is as follows.

Table 5. Measured, computed, and simulated differential pairs input offset voltages, for NMOS transistors of a given die.

	Measured		Computed		Simulated (method 1)		Simulated (method 2)	
Sizes	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=0V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=1V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=0V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=1V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=0V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=1V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=0V)$	$\sigma_{(V_{offset})^{(mV)}}$ $(V_{SB}=1V)$
40/40	1.3041	1.2369	1.281	1.235	1.90	1.69	1.4077	1.3548
40/10	3.1648	2.9778	3.128	2.984	2.67	2.33	3.2888	3.2454
40/4	4.4083	4.0222	4.296	4.036	4.41	3.90	4.4711	4.4122
40/2	5.7135	5.3017	5.575	5.401	7.80	6.99	5.4023	5.7256
40/1	12.1122	13.5417	12.575	14.079	17.29	15.68	14.0158	15.6491
20/40	2.5320	2.2303	2.528	2.265	2.20	1.91	2.5584	2.1511
20/10	2.9655	2.7695	2.931	2.763	3.29	2.84	3.1032	3.0614
20/4	5.2575	4.7859	5.194	4.817	5.44	4.77	5.2443	5.2064
20/2	8.3418	7.2832	8.279	7.407	9.41	8.39	7.8699	7.6360
20/1	20.8098	21.4372	21.110	22.027	20.20	18.28	23.1603	24.8110
10/40	1.8492	1.7251	1.830	1.712	2.87	2.46	1.8822	1.7797
10/10	6.6207	5.7666	6.504	5.829	4.31	3.70	6.6108	5.6031
10/4	8.8444	7.5801	8.744	7.698	7.02	6.12	9.0321	8.3982
10/2	10.7789	9.9204	10.442	9.896	11.87	10.52	10.3967	11.0116
10/1	24.4874	25.9678	24.572	26.831	24.77	22.37	27.1192	31.2029
5/40	3.9449	3.4340	3.921	3.481	4.32	3.66	4.1702	3.7580
5/10	5.4351	4.7066	5.328	4.715	6.01	5.10	5.5696	5.0075
5/4	8.7256	7.6528	8.694	7.695	9.29	8.02	8.6510	7.5812
5/2	17.7500	16.1167	17.645	16.218	15.29	13.45	18.7622	18.7392
5/1	18.2999	18.6891	18.319	18.818	31.19	27.97	20.4303	23.7233
2.5/40	9.3857	8.0999	9.400	8.243	7.33	6.09	9.9110	9.0891
2.5/10	7.6850	6.9679	7.640	6.967	8.83	7.37	8.3719	7.9461
2.5/4	13.8047	12.0785	13.218	11.907	12.29	10.47	14.7429	13.5792
2.5/2	15.6288	14.2745	15.825	14.497	19.30	16.84	16.1576	15.2941
2.5/1	30.0931	29.0792	30.247	29.488	38.67	34.35	32.7123	37.8362
1.25/40	11.6955	9.9583	11.749	10.190	13.28	10.66	12.8067	11.9650
1.25/10	16.4827	15.4563	16.428	15.305	13.68	11.07	19.3184	18.9713
1.25/4	14.9078	13.7128	14.526	13.417	15.61	13.04	16.4553	16.6279
1.25/2	22.2949	20.6132	21.782	20.573	21.83	19.02	24.1983	26.0047
1.25/1	33.3080	34.2983	34.300	34.713	42.60	37.61	40.0272	44.3559

Each transistor in the netlist is substituted by a subcircuit call which includes a MOS transistor of the specified size and whose β, V_{T0}, and γ are recomputed by adding noise to them. If $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{r0})}$, and $\sigma_{(\Delta\gamma)}$ are the interpolated functions for the deviations then the recomputed values for β, V_{T0}, and γ are,

$$\begin{aligned}
\beta_{new} &= \beta_{nominal} + \Delta\beta \\
\Delta\beta &= \beta_{nominal} GAUS\left(mean = 0, sigma = \frac{1}{\sqrt{2}}\sigma_{(\Delta\beta/\beta)}\right) \\
V_{T0_{new}} &= V_{T0_{nominal}} + \Delta V_{T0} \\
\Delta V_{T0} &= GAUS\left(mean = 0, sigma = \frac{1}{\sqrt{2}}\sigma_{(\Delta V_{T0})}\right) \\
\gamma_{new} &= \gamma_{nominal} + \Delta\gamma \\
\Delta\gamma &= GAUS\left(mean = 0, sigma = \frac{1}{\sqrt{2}}\sigma_{(\Delta\gamma)}\right)
\end{aligned} \tag{50}$$

where GAUS($\cdot$) is a normally distributed random number generation routine whose ''*mean*'' and ''*sigma*'' values have to be provided. Note that each deviation is divided by ''$\sqrt{2}$''. This is because the transistor defined by equation (50) is deviated with respect to a nominal one. Consequently, the mismatch in parameter P between two transistors, each deviated $\frac{1}{\sqrt{2}}\sigma_{(\Delta P)}$ from a nominal transistor, is $\sigma_{(\Delta P)}$. And it is this $\sigma_{(\Delta P)}$ that we have measured and characterized in the previous Sections. The HSPICE input file section that performs what describes equation (50) is:

```
.subckt nmod_typ Drain Gate Source Bulk width=w
length=l
m_nmod Drain Gate Source Bulk nmos w=w l=l
*
.MODEL NMOS NMOS
+ LEVEL   = 6.0     UPDATE = xxxxxxx
+ XL      = xxxxxxx WDEL   = xxxxxxx LATD   = xxxxxxx
+ VTO     = vto_n   TOX    = xxxxxxx BETA   = beta_n
+ GAMMA   = gamma_n VBO    = xxxxxxx LGAMMA = xxxxxxx
+ NWE     = xxxxxxx NWM    = xxxxxxx SCM    = xxxxxxx
+ FDS     = xxxxxxx UFDS   = xxxxxxx VFDS   = xxxxxxx
+ VSH     = xxxxxxx NSUB   = xxxxxxx XJ     = xxxxxxx
+ MOB     = xxxxxxx NU     = xxxxxxx
+ F1      = xxxxxxx F2     = xxxxxxx UTRA   = xxxxxxx
+ ECRIT   = xxxxxxx KU     = xxxxxxx
+ CLM     = xxxxxxx
+ MCL     = xxxxxxx KCL    = xxxxxxx
+ KA      = xxxxxxx MAL    = xxxxxxx
+ LAMBDA  = xxxxxxx MBL    = xxxxxxx
+ WIC     = xxxxxxx WEX    = xxxxxxx NSS    = xxxxxxx
+ NFS     = xxxxxxx
+ BEX     = xxxxxxx TCV    = xxxxxxx TLEV   = xxxxxxx
+ CJ      = xxxxxxx MJ     = xxxxxxx RSH    = xxxxxxx
+ CJSW    = xxxxxxx MJSW   = xxxxxxx PB     = xxxxxxx
+ CGDO    = xxxxxxx CGSO   = xxxxxxx JS     = xxxxxxx

*
.param beta_n_global_typ=xxxxxxx
.param vto_n_global_typ=xxxxxxx
.param gamma_n_global_typ=xxxxxxx
*
.param sigma_fit_beta = 'C00_beta+C01_beta/(w-Ew_beta)
+C10_beta/(L-El_beta) + ...'
.param sigma_fit_vto = 'C00_vto+C01_vto/(w - Ew_vto)
+C10_vto/(L - El_vto) + ...'
.param sigma_fit_gamma = 'C00_gamma+C01_gamma/(w - Ew_gamma)
+C10_gamma/(L - El_gamma) + ...'
*
.param sigma_beta = 'sigma_fit_beta/1.414213562'
.param sigma_vto = 'sigma_fit_vto/1.414213562'
.param sigma_gamma = 'sigma_fit_gamma/1.414213562'
*
.param delta_beta=agauss(0,sigma_beta,1)
.param delta_vto=agauss(0,sigma_vto,1)
.param delta_gamma=agauss(0,sigma_gamma,1)
*
.param beta_n = 'beta_n_global_typ*(1+delta_beta)'
.param vto_n = 'vto_n_global_typ+delta_vto'
.param gamma_n = 'gamma_n_global_typ+delta_gamma'
.ends
```

The values for $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$, and $\sigma_{(\Delta\gamma)}$ have to be provided for each transistor size using, for example, a nonlinear interpolation like in equation (37). Using this procedure the differential pairs input offset voltages described in Section 5.C. were simulated for all transistor sizes, with and without substrate effect. The results are given in Table 5 under the columns named ''Simulated (method 1)''.

B. Method 2

The previous method has two problems:

- The MOS transistor model provided by the manufacturer might not include some of the large signal parameters we have used, like β, V_{T0}, θ or γ.
- The physical meaning of parameters β, V_{T0}, θ or γ in the MOS model provided by the manufacturer (if they are present) is probably different to the one in the model we have assumed (and used in equations (8)–(10)). Therefore, Method 1 is only an approximate procedure for predicting transistor mismatch, and this method might produce good or bad results depending on how much the transistor model provided by the manufacturer differs from the one we have assumed.

A possible alternative to overcome these problems would be to substitute each transistor in the netlist by the subcircuit depicted in Fig. 12. The subcircuit includes 3 MOS transistors and a set of controlled sources. Transistor M_{MAIN} is a nominal transistor (without deviations) using the model provided by the

manufacturer. Transistors m_{nom} and m_{dev} are modeled using the transistor model we have assumed (equations (8)–(10)). Transistor m_{nom} is a nominal transistor and transistor m_{dev} is such that its β, V_{T0}, θ and γ values are modified by adding random deviations. The voltage controlled voltage sources that bias transistors m_{nom} and m_{dev} do the function of copying the terminal voltages present at transistor M_{MAIN}. The currents flowing through each transistor are sensed: I_{DS} for M_{MAIN}, I_1 for m_{nom}, and I_2 for m_{dev}. Transistor M_{MAIN} has a current source in parallel ΔI_{DS} whose value at each instant is given by

$$\Delta I_{DS} = I_{DS}\frac{I_1 - I_2}{I_1} \tag{51}$$

Note that now we can use our five *mismatch parameter* $\{\Delta\beta/\beta,\ \Delta V_{T0},\ \Delta\theta_o,\ \Delta\theta_e,\ \Delta\gamma\}$ model to define the *large signal parameters* for m_{dev}. The goal is to be able to generate for each m_{dev} these 5 *mismatch parameters* by knowing their standard deviations and respective correlation coefficients. This can be done in (H)Spice as follows. Suppose that for each m_{dev} transistor we know its *statistical mismatch parameters* (i.e. equations (34)–(35)), obtained for example using the information in Table 3 or Table 4. Suppose also, that for each m_{dev} we can generate 5 random number $\{x_1, x_2, x_3, x_4, x_5\}$ which are uncorrelated, have zero mean, and their standard deviation is $\sigma(x_i) = 1/\sqrt{2}$. Using these five uncorrelated random numbers we can obtain five correlated mismatch parameters for m_{dev} as follows,

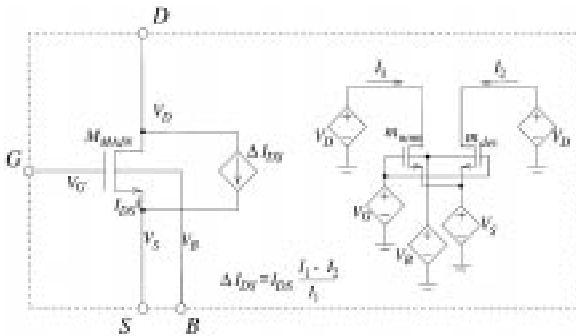

Fig. 12. MOS transistor subcircuit substitution for *Method 2* mismatch simulations.

$$\begin{aligned}
\Delta\beta/\beta &= c_{11}x_1 \\
\Delta V_{T0} &= c_{21}x_1 + c_{22}x_2 \\
\Delta\theta_o &= c_{31}x_1 + c_{32}x_2 + c_{33}x_3 \\
\Delta\theta_e &= c_{41}x_1 + c_{42}x_2 + c_{43}x_3 + c_{44}x_4 \\
\Delta\gamma &= c_{51}x_1 + c_{52}x_2 + c_{53}x_3 + c_{54}x_4 + c_{55}x_5
\end{aligned} \tag{52}$$

By computing the standard deviations of the right and left hand side of equation (52), as well as those of pairwise sums of these equations, all coefficients c_{ij} can be obtained,

$$\begin{aligned}
&c_{11} = \sigma_\beta \rightarrow c_{21} = r_{\beta V_{T0}}\sigma_{V_{T0}} \rightarrow c_{22}^2 = \sigma_{V_{T0}}^2 - c_{21}^2 \\
&c_{31} = r_{\beta\theta_o}\sigma_{\theta_o} \rightarrow c_{32} = \frac{r_{V_{T0}\theta_o}\sigma_{V_{T0}}\sigma_{\theta_o} - c_{21}c_{31}}{c_{22}} \rightarrow \\
&c_{33}^2 = \sigma_{\theta_o}^2 - c_{31}^2 - c_{32}^2 \\
&c_{41} = r_{\beta\theta_e}\sigma_{\theta_e} \rightarrow c_{42} = \frac{r_{V_{T0}\theta_e}\sigma_{V_{T0}}\sigma_{\theta_e} - c_{21}c_{41}}{c_{22}} \rightarrow \\
&c_{43} = \frac{r_{\theta_o\theta_e}\sigma_{\theta_o}\sigma_{\theta_e} - c_{31}c_{41} - c_{32}c_{42}}{c_{33}} \rightarrow \\
&c_{44}^2 = \sigma_{\theta_e}^2 - c_{41}^2 - c_{42}^2 - c_{43}^2 \\
&c_{51} = r_{\beta\gamma}\sigma_\gamma \rightarrow c_{52} = \frac{r_{V_{T0}\gamma}\sigma_{V_{T0}}\sigma_\gamma - c_{21}c_{51}}{c_{22}} \rightarrow \\
&c_{53} = \frac{r_{\theta_o\gamma}\sigma_{\theta_o}\sigma_\gamma - c_{31}c_{51} - c_{32}c_{52}}{c_{33}} \rightarrow \\
&c_{54} = \frac{r_{\theta_e\gamma}\sigma_{\theta_e}\sigma_\gamma - c_{41}c_{51} - c_{42}c_{52} - c_{43}c_{53}}{c_{44}} \rightarrow \\
&c_{55}^2 = \sigma_\gamma^2 - c_{51}^2 - c_{52}^2 - c_{53}^2 - c_{54}^2
\end{aligned} \tag{52}$$

The value for $\Delta\theta_{eff}$ is explicitly computed as

$$\begin{aligned}
\Delta\theta_{eff} &= \Delta\theta_o + f(V_{GS'}V_{DS'}V_T) \times \Delta\theta_e \\
f(V_{GS'}V_{DS'}V_T) &= \frac{V_{DS}}{V_{GS} - V_T}\frac{1}{1 + e^{\frac{V_{DS}-V_{GS}-V_T}{V_\varepsilon}}} + \frac{1}{1 + e^{-\left(\frac{V_{DS}-V_{GS}-V_T}{V_\varepsilon}\right)}}, \\
V_\varepsilon &= 1\,\text{mV}
\end{aligned} \tag{54}$$

to assure that in ohmic region $\Delta\theta_{eff} = \Delta\theta_o + \Delta\theta_e(V_{DS}/(V_{GS} - V_T))$, and in saturation $\Delta\theta_{eff} = \Delta\theta_o + \Delta\theta_e$. This way, the following (H)Spice subcircuit call can be used for the circuit in Fig. 12.

```
.subckt nmod Drain Gate Source Bulk width = w length = 1
*
.param x01 = agauss (0,0.7071,1)
.param x02 = agauss (0,0.7071,1)
.param x03 = agauss (0,0.7071,1)
.param x04 = agauss (0,0.7071,1)
.param x05 = agauss (0,0.7071,1)
.param x1 = x01
.param x2 = x02
.param x3 = x03
.param x4 = x04
.param x5 = x05
*
.param a1 =' c11*x1'
.param a2 =' c21*x1 + c22*x2'
.param a3 =' c31*x1 + c32*x2 + c33*x3'
.param a4 =' c41*x1 + c42*x2 + c43*x3 + c44*x4'
.param a5 =' c51*x1 + c52*x2 + c53*x3 + c54*x4 + c55*x5'
*
.model nmod_nom nmos level = 1 kp =' beta' vto =' vto'phi =' phi'
+ lambda = 0.0 gamma =' gamma' delta = 0 nsub = 1e30 ucrit = 0
*
m_main Drain Gate Source_2 Bulk nmod_manufacturer w = w 1 = 1
vnull Source_2Source 0
m_aux_nom D1aux Gaux Saux Baux nmod_nom
m_aux_dev D2aux Gaux Saux Baux nmod_ext
eg_aux Gaux 0 Gate 0 1
ed1_aux D1aux dd1 Drain 0 1
vdd1 dd1 0 0
ed2_aox D2aux dd2 Drain 0 1
vdd2 dd2 0 0
es_aux Saux 0 Source 0 1
eb_aux Baux 0 Bulk 0 1
e_sigm1 sigm1 0 vol =' 1/(1 + exp ((v(Drain) -v (Gate) + v(vt))/0.001))'
e_sigm2 sigm2 0 vol = '1/(1 + exp(-(v(Drain) - v(Gate) + v (vt))/0.001))'
e_vsat fsat 0 vol = '(v(Drain) - v(Source))/(v(Gate) - v(Source) - v(vt))*v (sigm1) + v(sigm2)'
evt vt 0 vol =' vto + gamma*(sqrt(v(Saux) - phi) - sqrt(phi))'
e_deltai n1 0 vol = '(i(vdd1) -i (vdd2)*((1 + theta*(v(Gaux) - v(Saux) - v(vt)))/(1 + (theta + a3+
v(fsat)*a4)*(v(Gaux) - v(Saux) - v(vt)))))/i(vdd1)*i (vnull)'
g_deltai Drain Source n1 0 1
*
.model nmod_ext nmos level = 1 kp =' beta*(1 + a1)' vto = 'vto + a2' phi =' phi'
+ lambda = 0.0 gamma =' gamma + a5' delta = 0nsub = 1e30 ucrit = 0
.ends
```

Using the set-up on page 296, and performing Monte Carlo simulations to predict the differential pair input offset voltages for each transistor size, with and without substrate effect, results in the values shown in Table 5 under the columns named ''Simulated (method 2)''. Note that these values are more similar to those shown in Table 5 under columns named ''Computed'' than the ones obtained with the first method of simulation. However, the values under ''Simulated (method2)'' and ''Computed'' are not identical. The reason is that the coefficient I_{DS}/g_m of equation (49) is computed by the simulator using the manufacturer transistor model (through transistor M_{MAIN}), instead of the one we have assumed (i.e. equations (8)–(10)).

7. Conclusions

A MOS transistor mismatch characterization technique has been developed that enables circuit designers to perform this task at low costs. The technique is based on the design of a special purpose chip that includes a wide range of transistor sizes. A new transistor mismatch model is proposed based on five mismatch parameters. These mismatch parameters are unique for each transistor and valid for ohmic and saturation regions (both for strong inversion). The technique has been used to characterize a digital $1.0\,\mu$m CMOS technology. Mismatch data has been extracted and modeled through interpolation surfaces that depend on tran-

sistor width W and length L. The correctness of the extracted mismatch data has been checked by predicting differential pairs input offset voltages, and the interpolation surfaces have been used in conventional electrical circuit simulators to model transistor mismatch. Experimental and simulated data agree very well.

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Notes

1. Sometimes manufacturers provide mismatch information as a function of transistor area, but this information is usually obtained for (almost) square transistors only [6].
2. This phenomenon is caused by the topographic fact that transistors in the periphery of an array ''see'' a different vecinity than those not on the periphery [13,20]. It is a well known phenomenon among analog circuit designers and can be avoided by adding dummy cells surrounding an array.
3. It should be mentioned here that in general any physical phenomenon introducing a systematic component (such as a gradient plane) may introduce an extra random variation. Since the gradient-induced mismatch contribution to ΔP increases with distance, its associated extra random variation might also depend on distance. However, this is not the main contribution to the S_p term in equation (2) and should be regarded as a high order effect, which we are ignoring in this paper.
4. All voltages and currents are taken in absolute value, so that the same expressions are valid for NMOS and PMOS transistors.
5. In the particular case of our instrument (HP4145) we also had to turn off the auto-calibration feature, so that the instrument would not calibrate between steps 2.1 and 2.2, which may introduce an artificial offset.
6. A circuit designer might be tempted to cancel out the third term in equation (19) by adjusting l_d. However, note that canceling this term does not eliminate $\Delta\theta_e$ in equation (20), since v_s is not 100% correlated to $C_{ox}\ l_d\ R_\square$.
7. Values for β are different in saturation than in ohmic: $\beta_{sat} = \beta_{ohm}/(1+\delta)$ [18]. However, $\Delta\beta/\beta$ will be identical for both regions, assuming $\Delta\ \delta$ is negligible.
8. The chips yielding the minimum and maximum mismatch were not the same for all transistor sizes.
9. In the same way many silicon foundries provide a ''*typical*'', ''*slow*'', and ''*fast*'' model for the transistor large signal model.
10. To our surprise, size 40/2 was more difficult to fit to the models than size 40/1.
11. We verified empirically that this weight provided good results. The numerator makes the weight to become rapidly negligible for large Ω_i values, while the denominator assures a very high weight for close-to-zero values.
12. To our knowledge, this excellent agreement between measured and predicted mismatches has never been reported in the open literature for such a wide range of transistor sizes. Usually a 20% error is considered to be a good approximation.

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