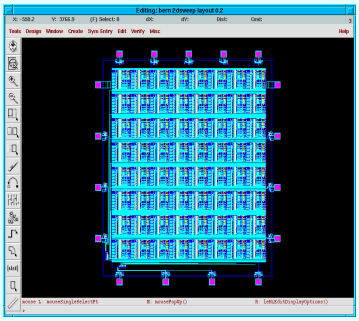
CMOS Processes Mismatch Characterization Consulting Service

The National Microlectronics Center (IMSE - CNM - CSIC) has developed a CMOS process mismatch characterization methodology, which allows to predict and simulate transistor mismatch behavior as a function of its width and length. The method does not require special equipment (no expensive probing setups), but only a computer and a precise means for measuring I/V curves.

This simple mismatch characterization methodology turned out to be fairly robust and efficient. As a result, IMSE has developed a new mismatch model, which predicts transistor mismatch for any transistor size with better precision.

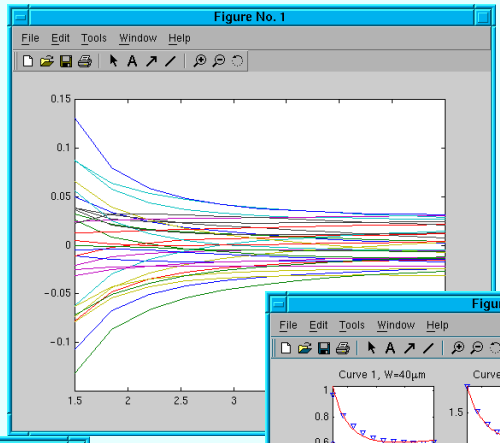
IMSE offers its expertize and software to world wide companies, institutions and universities interested in having a good transistor mismatch characterization of the VLSI processes they use. The mismatch characterization procedure involves several steps, as described below, that can be independently contracted.



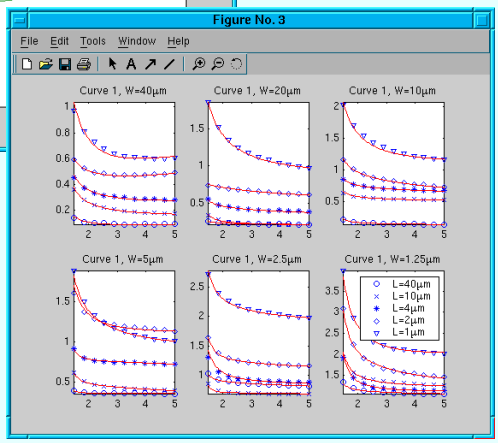
A special purpose chip is designed, containing an array of identical cells. Each cell contains different NMOS and PMOS transistors of different sizes (typically 30). A special decoding circuitry technique allows to access individually each transistor from the same sensing pins. A conventional I/V measuring instrument is required. The chip contains several thousands of transistors, which are typically measured in 20-30 hours.

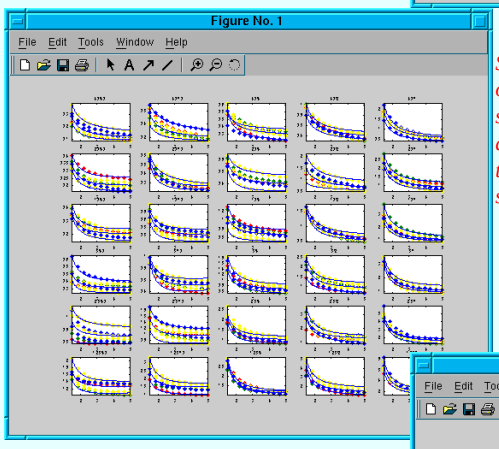
The different steps of the mismatch characterization procedure are:

- STEP 1: *Chip Design.* Design of a special purpose chip to measure CMOS transistor mismatch behavior for a wide variety of transistor sizes (typically 30). This allows to sample properly the transistor sizing design space (1/*W*, 1/*L*).
- *STEP 2: Intensive Measurements.* Measurement of a minimum set of *I*/*V* curves per transistor pair, which allows to predict transistor mismatch for a wide range of biasing points. To characterize mismatch, only a small number of chips is required (typically around 10).
- *STEP 3: Data Processing.* A MATLAB based software is provided which performs the following functions. (1) Extraction of a minimum set of mismatch parameters that fully characterize mismatch behavior for a wide range of biasing points. (2) Computation of statistical parameters to predict behavior of mismatch parameters as a function of transistor sizing.
- *STEP 4: Simulation.* Implementation of the model in standard electrical circuit simulators (Hspice) to predict transistor mismatch as a function of length and width.



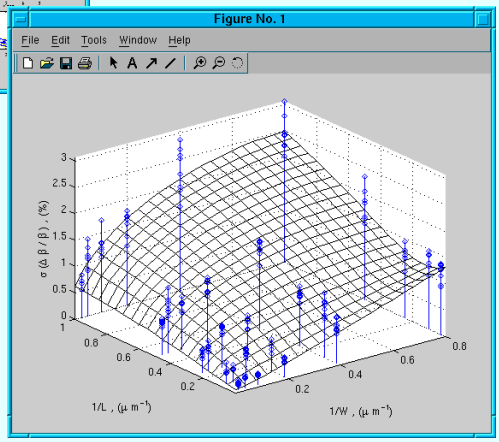
Measured $\Delta I_{DS}/I_{DS}$ for 30 different NMOS minimum size transistor pairs in saturation. The procedure requires to measure 4 (two in ohmic and two in saturation) different mismatch curves for each transistor pair.

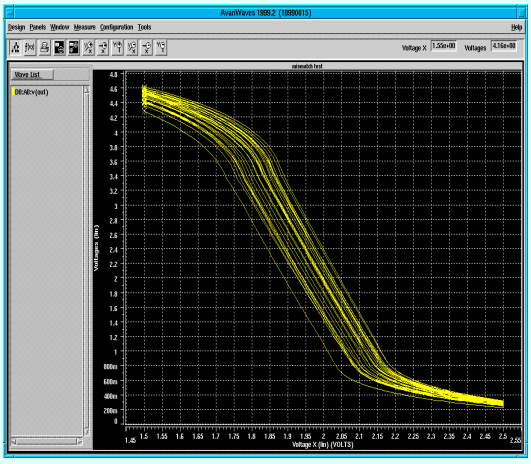




Spread over several dies for all transistor sizes

Measured vs. predicted standard deviation for mismatch currents. for 30 transistor sizes.





By properly including the mismatch model in a standard (Hspice) circuit simulator, using all derived fitting functions for statistical mismatch parameters, mismatch can be easily simulated for any combination of transistor width (W) and length (L).

Each mismatch parameter is obtained for a wide range of transistor sizes. This allows a good sampling of the complete transistor sizing space (1/W,1/L), and the construction of a fitting surface to properly predict the mismatch parameter for any transistor size.

References:

(available from `http://www.imse.cnm.es/~mismatch`)

- Teresa Serrano-Gotarredona and Bernabé Linares-Barranco, "A New 5-Parameter MOS Transistor Mismatch Model," *IEEE Electron Device Letters*, vol. 21, No. 1, pp. 37-39. January 2000.
- Teresa Serrano-Gotarredona and Bernabé Linares-Barranco, "Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation," *Journal of Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers, vol. 21, No. 3, pp. 271-296, December 1999.
- T. Serrano-Gotarredona and B. Linares-Barranco, "A 5-Parameters Mismatch Model for Short Channel MOS Transistors," *Proceedings of the 1999 European Solid State Circuits Conference* (ESSCIRC99), pp. 440-443, 1999.

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